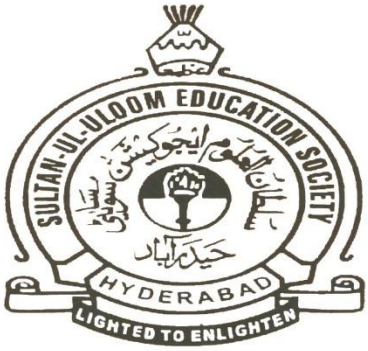
MUFFAKHAM JAH
COLLEGE OF ENGINEERING AND TECHNOLOGY

# PC551EC INTEGRATED CIRCUITS LAB

*(With effect from the academic year 2016-2017)*

## STUDENT'S MANUAL




**DEPARTMENT OF**
**ELECTRONICS AND COMMUNICATION ENGINEERING**

## Vision and Mission of the Institution

### Vision

To be part of universal human quest for development and progress by contributing high calibre, ethical and socially responsible engineers who meet the global challenge of building modern society in harmony with nature.

### Mission

- To attain excellence in imparting technical education from the undergraduate through doctorate levels by adopting coherent and judiciously coordinated curricular and co-curricular programs
- To foster partnership with industry and government agencies through collaborative research and consultancy
- To nurture and strengthen auxiliary soft skills for overall development and improved employability in a multi-cultural work space
- To develop scientific temper and spirit of enquiry in order to harness the latent innovative talents
- To develop constructive attitude in students towards the task of nation building and empower them to become future leaders
- To nourish the entrepreneurial instincts of the students and hone their business acumen.
- To involve the students and the faculty in solving local community problems through economical and sustainable solutions.

## Vision and Mission of ECE Department

### Vision

To be recognized as a premier education center providing state of art education and facilitating research and innovation in the field of Electronics and Communication.

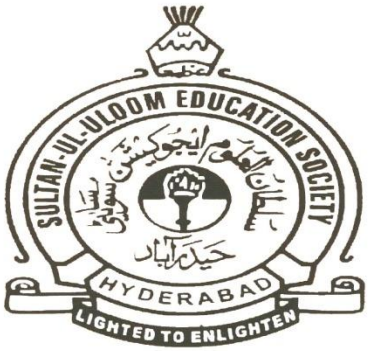
### Mission

We are dedicated to providing high quality, holistic education in Electronics and Communication Engineering that prepares the students for successful pursuit of higher education and challenging careers in research, R& D and Academics.

### Program Educational Objectives of B. E (ECE) Program:

1. Graduates will demonstrate technical competence in their chosen fields of employment by identifying, formulating, analyzing and providing engineering solutions using current techniques and tools
2. Graduates will communicate effectively as individuals or team members and demonstrate leadership skills to be successful in the local and global cross-cultural working environment
3. Graduates will demonstrate lifelong learning through continuing education and professional development
4. Graduates will be successful in providing viable and sustainable solutions within societal, professional, environmental and ethical contexts

**MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY**
**BANJARA HILLS, ROAD NO-3, TELANGANA**




# LABORATORY MANUAL

# FOR

# INTEGRATED CIRCUITS LAB

**Prepared by:**

**Checked by:**

**Approved by:**

# MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY

## DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

**(Name of the Subject/Lab Course): Integrated Circuits Lab**

**Code: EC331** **Programme: UG**

**Branch: ECE** **Version No: 1**

**Year : III** **Updated on: 20/3/16**

**Semester :I** **No. of Pages:**

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**3)Designation :** **2) Sign :**

**4) Date :** **3) Designation :**

**4) Date :**

**Approved by: (HOD) 1) Name:**

**2) Sign :**

**3) Date :**

## INTEGRATED CIRCUITS LAB

| | |
|---|---|
| Instruction | 3 Periods per week |
| Duration of University Examination | 3 Hours |
| University Examination | 50 Marks |
| Sessional | 25Marks |

***Lab Experiments:***

### Part-A

1. Measurement of parameters of Op-Amp. Voltage Follower, Inverting and Non Inverting Amplifiers, Level Translators using Op-Amp.
2. Arithmetic Circuits: Summer, Integrator Differentiator Op-Amp.
3. Active filters: LP, HP and BP using Op-Amp.
4. Op-Amp Oscillators: Astable, Monostable.
5. Triangle and Square wave Generators. Schmitt Trigger using Op-Amp.
6. Voltage Controlled Oscillator Using LM 566.
7. IC Regulators and current boosting.
8. Applications of 555 Timer.

### Part-B

1. Measurement of propagation delay, fan-out, Noise margin and transfer Characteristics of TTL and CMOS IC gates and open collector / drain gates.
2. Designing code converters using logic gates and standard code converters. Parity generator and checker circuit.
3. Flip-Flop conversions and latches using gates and ICs.
4. Designing Synchronous, Asynchronous up/down counters
5. Shift registers and ring counters using IC Flip-Flops & Standards IC counters.
6. Full adders, subtractors using logic gates and multiple bits IC Adder/ Subtractor and arithmetic Circuits.
7. Mux - Demux applications.
8. Interfacing counters with 7-segment LED/LCD display units.

**General Note:**

1. At least 5 experiments from each part.

2. A total of not less than 10 experiments must be carried out during the semester.
3. Analysis and design of circuits, wherever possible, should be carried out using SPICE tools.

## ANALOG ELECTRONICS AND INTEGRATED CIRCUITS LAB GENERAL GUIDELINES AND SAFETY INSTRUCTIONS

1. Sign in the log register as soon as you enter the lab and strictly observe your lab timings.
2. Strictly follow the written and verbal instructions given by the teacher / Lab Instructor. If you do not understand the instructions, the handouts and the procedures, ask the instructor or teacher.
3. **Never work alone!** You should be accompanied by your laboratory partner and / or the instructors / teaching assistants all the time.
4. It is mandatory to come to lab in a formal dress and wear your ID cards.
5. Do not wear loose-fitting clothing or jewellery in the lab. Rings and necklaces are usual excellent conductors of electricity.
6. Mobile phones should be switched off in the lab. Keep bags in the bag rack.
7. Keep the labs clean at all times, no food and drinks allowed inside the lab.
8. Intentional misconduct will lead to expulsion from the lab.
9. Do not handle any equipment without reading the safety instructions. Read the handout and procedures in the Lab Manual before starting the experiments.
10. Do your wiring, setup, and a careful circuit checkout before applying power. Do not make circuit changes or perform any wiring when power is on.
11. Avoid contact with energized electrical circuits.
12. Do not insert connectors forcefully into the sockets.
13. **NEVER** try to experiment with the power from the wall plug.
14. Immediately report dangerous or exceptional conditions to the Lab instructor / teacher: Equipment that is not working as expected, wires or connectors are broken, the equipment that smells or "smokes". If you are not sure what the problem is or what's going on, switch off the Emergency shutdown.
15. Never use damaged instruments, wires or connectors. Hand over these parts to the Lab instructor/Teacher.
16. Be sure of location of fire extinguishers and first aid kits in the laboratory.
17. After completion of Experiment, return the bread board, trainer kits, wires, CRO probes and other components to lab staff. Do not take any item from the lab without permission.
18. Observation book and lab record should be carried to each lab. Readings of current lab experiment are to be entered in Observation book and previous lab experiment should be written in Lab record book. Both the books should be corrected by the faculty in each lab.
19. Handling of Semiconductor Components:Sensitive electronic circuits and electronic components have to be handled with great care. The inappropriate handling of electronic component can damage or destroy the devices. The devices can be destroyed by driving to high currents through the device, by overheating the device, by mixing up the polarity, or by electrostatic discharge (ESD). Therefore, always handle the

electronic devices as indicated by the handout, the specifications in the data sheet or other documentation.

20. Special Precautions during soldering practice
    a. Hold the soldering iron away from your body. Don't point the iron towards you.
    b. Don't use a spread solder on the board as it may cause short circuit.
    c. Do not overheat the components as excess heat may damage the components/board.
    d. In case of burn or injury seek first aid available in the lab or at the college dispensary

# LIST OF EXPERIMENTS

## PART-A

**List of Experiments** **Pg.No**



## PART-B

# PART-A

# Experiment 1

## Measurements of OP-AMP parameters and Basic Applications

### (A). Measurements of OP-AMP parameters

**AIM:**

(A).To measure the following parameters of op-amp

1. Input bias current
2. Input offset current
3. Input and Output offset voltage
4. Slew rate

(B). Basic Applications

1. To design an amplifier with gain of -10.
2. To design an amplifier with gain of 11.
3. To realize a voltage follower using op-amp.

**APPARATUS REQUIRED**:

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- µA741C | 1 |
| Resistor-100Ω | 2 |
| Resistor-10k | 2 |
| Resistor-100k | 1 |
| Capacitors-0.01µF | 2 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Digital ammeter | 0-200µA/200mA | 1 |
| Digital voltmeter | 0-2V/20V | 1 |
| Function generator | 0-20MHz. | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:**

The µA741 device is a general-purpose operational Short-Circuit Protection amplifier featuring offset-voltage null capability.

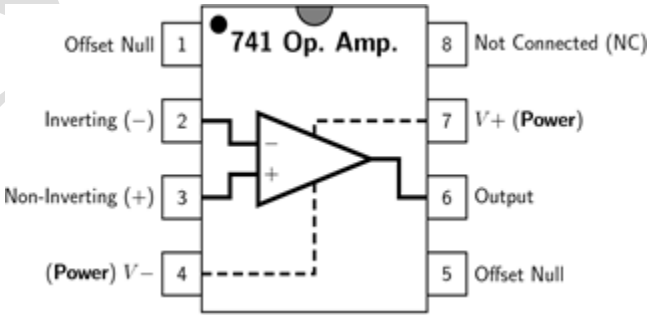
**Input bias current:** The inverting and noninverting terminals of an op-amp are actually two base terminals of transistors of a differential amplifier. In an ideal op-amp it is supported that no current flows through these terminals. However, practically a small amount of current flows through these terminals which is on the order of nA (typical and maximum values are 80 and 1500nA) in bipolar op-amps and pA for FET op-amps. Input bias current is defined as the average of the currents entering into the inverting and noninverting terminals of an op-amp. To compensate for bias currents a compensating resistor Rcomp is used. Value of Rcomp is parallel combination of the resistors connected to the inverting terminal. Input bias current $I_B=(I_{B1}+I_{B2})/2$ where $I_{B1}$ and $I_{B2}$ are the base bias currents of the op-amp.

**Input offset current:** The bias currents IB1 and IB2 will not be equal in an op-amp. Input offset current is defined as the algebraic difference between the currents into the inverting and non-inverting terminals. $Ios=|I_{B1}-I_{B2}|$ Typical and maximum values of input offset current are 20nA and 200nA.

**Input offset voltage:** Even if the input voltage is zero, output voltage may not be zero. This is because of the circuit imbalances inside the op-amp. In order to compensate this, a small voltage should be applied between the input terminals. Input offset voltage is defined as the voltage that must be applied between the input terminals of an op-amp to nullify the output voltage. Typical and maximum values of input offset voltage are 2mV and 6mV.

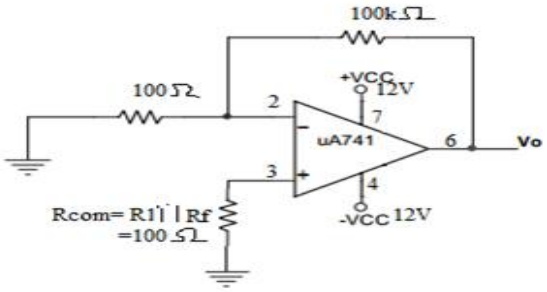
**Slew rate:** Slew rate is the rate of rise of output voltage. It is the measure of fastness of op-amp. It is expressed in V/μsec. If the slope requirements of the output voltage of the op-amp are greater than the slew rate, distortion occurs. Slew rate is measured by applying a step input voltage.

**PIN DIAGRAM:**



**CIRCUIT DIAGRAM:**

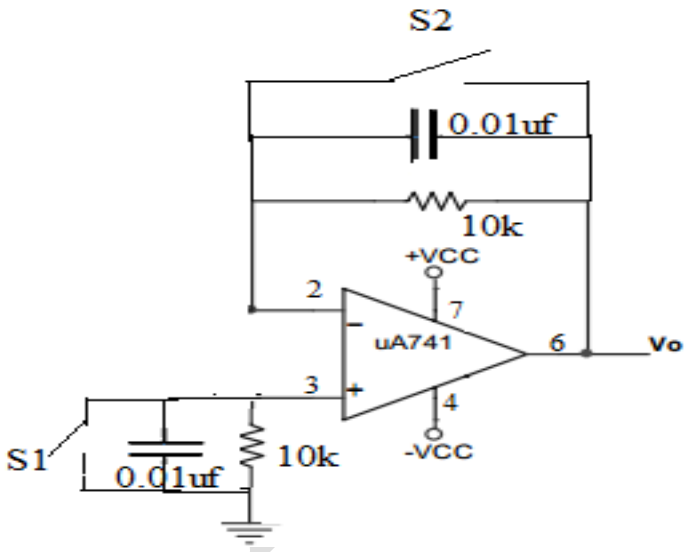
**To Measure Output and Input offset voltage**




**Procedure:-**

1. Connect the circuit as shown in figure and measure Output voltage i.e; Output offset voltage ($V_{oo}$).
2. Calculated Input offset voltage from
   $V_{io}$= $Voo/((I + Rf/R1)$.

**To measure Input bias current and Input offset current**

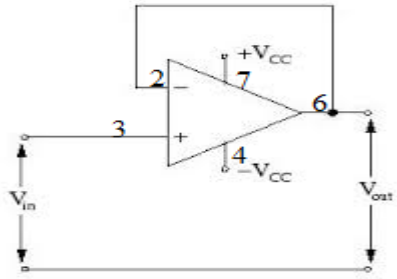


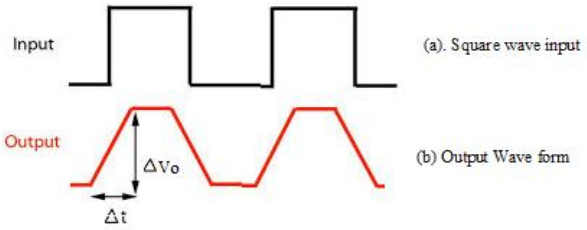

**Procedure:-**

1. Connect the circuit as shown in above figure.Closes switch S1 and measure Output voltage.
2. From output voltage calculate $I_{B2}$
   $I_{B2}$ = $Vo_2$/10K
3. Now Close S2 and Measure Output voltage.
4. From output voltage calculate $I_{B1}$
   $I_{B1}$ = $Vo_1$/10K.

5. From $I_{B1}$& $I_{B2}$ calculate Input bias current and Input offset current.
   $I_B=|I_{B1}+I_{B2}|/2$;
   Iio $=|I_{B1}| -|I_{B2}|$;

To measure slew rate




Procedure:-

1. Connect unity gain amplifier circuit and apply 1V(p-p) and 1 Khz freq Square wave as input .
2. Observe Output waveform at higher frequencies by varying freq of input from 1khz to higher value.
3. Slew rate can be calculated
   Slew Rate = $\Delta Vo/\Delta t$

**Observations& Calculations:**

1. Voo=…….

` Vio=Voo/(1+Rf/R1)

2. $Vo_2$=……..

   $I_{B2}$ = Vo/10K
   $Vo_1$=……
   $I_{B1}$ = $Vo_1$/10K.
   $I_B=|I_{B1}+I_{B2}|/2$
   Iio $=|I_{B1}| -|I_{B2}|$

3. ΔVo=……..V
   Δt=……µsec
   Slew rate=…….

**RESULT:**

The input bias current, input offset current, input offset voltage and slew rate of the op-amp were determined.

Input offset voltage = ……..mV

Input bias current = ……..A

Input offset current = ...…...A

Slew rate = ……..V/µs.

## (B) Basic Applications

## AIM:-

1. To design an amplifier with gain of -10.
2. To design an amplifier with gain of 11.
3. To realize a voltage follower using op-amp.

**APPARATUS REQUIRED**:

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- µA741C | 1 |
| Resistor-100Ω | 2 |
| Resistor-10k | 1 |
| Resistor-100k | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:**

**INVERTING AMPLIFIER: -**In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal"and that "V1 always equals V2". However, in real world op-amp circuits both of these rules are slightly broken.

This is because the junction of the input and feedback signal is at the same potential as the positive ( + ) input which is at zero volts or ground then, the junction is a **"Virtual Earth"**. Because of this virtual earth node the input resistance of the amplifier is equal to the value of the input

resistor, Rin and the closed loop gain of the inverting amplifier can be set by the ratio of the two external resistors.

**DESIGN:-**

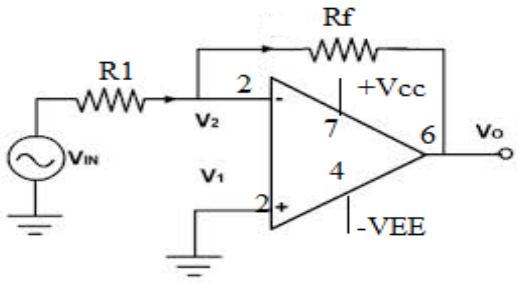
Gain of an inverting Amplifier is given by

Av=Vo/ Vin = -Rf/R1

Gain is given as -10

Let R1=10Kohm

Rf = Av.R1=> Rf = 100Kohm.




**PROCEDURE:-**

1. Connect the Circuit shown in above figure and Apply 1V(p-p) and 1 KHz sine wave as input .
2. Observe the output wave and calculate the gain of the amplifier practically.

**NON INVERTING AMPLIFIER:-**

The second basic configuration of an operational amplifier circuit is that of a Non-inverting Operational Amplifier. In this configuration, the input voltage signal, ( Vin ) is applied directly to the non-inverting ( + ) input terminal which means that the output gain of the amplifier becomes "Positive" in value in contrast to the "Inverting Amplifier" circuit we saw in the last tutorial whose output gain is negative in value. The result of this is that the output signal is "in-phase" with the input signal.

**DESIGN:-**

Gain of an inverting Amplifier is given by

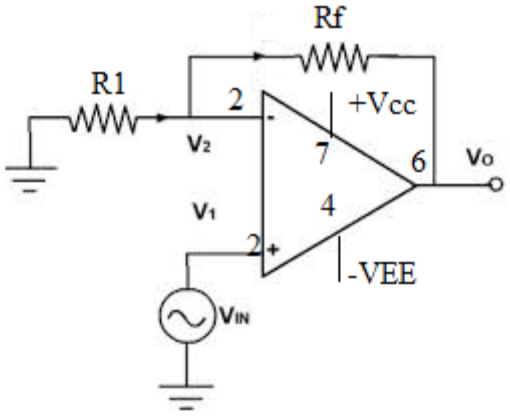
Av=Vo/ Vin = 1+Rf/R1

Gain is given as 11

Let R1=10Kohm

Rf = (Av-1).R1

⇨ Rf = 100Kohm




**PROCEDURE:-**

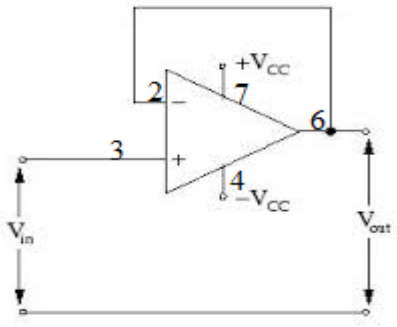
a. Connect the Circuit shown in above figure and Apply 1V(p-p) and 1 Khz sine wave as input .

b. Observe the output wave and calculate the gain of the amplifier practically.

**VOLTAGE FOLLOWER :-**

If we made the feedback resistor, R*f* equal to zero, (R*f* = 0), and resistor R1 equal to infinity, (R1 = ∞), then the circuit would have a fixed gain of "1" as all the output voltage would be present on the inverting input terminal (negative feedback). This would then produce a special type of the non-inverting amplifier circuit called a **Voltage Follower** or also called a "unity gain buffer".

As the input signal is connected directly to the non-inverting input of the amplifier the output signal is not inverted resulting in the output voltage being equal to the input voltage, Vout = Vin. This then makes the **voltage follower** circuit ideal as a **Unity Gain Buffer** circuit because of its isolation properties.




**PROCEDURE:-**

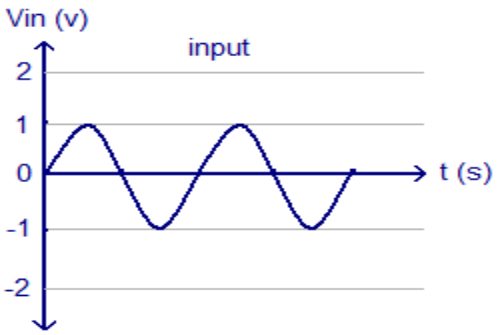
a. Connect the Circuit shown in above figure and Apply 1V(p-p) and 1 Khz sine wave as input.

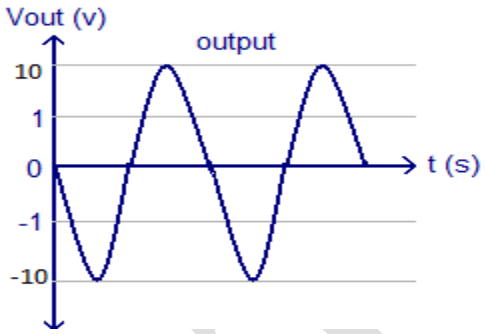
b. Measure the output.Vo=Vin

**Observations& Calculations:**

Input and Output wave forms for op-amp Inverting amplifier (Gain-10)

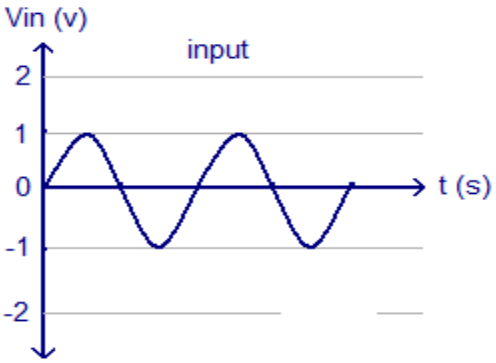
Av=Vo/ Vin

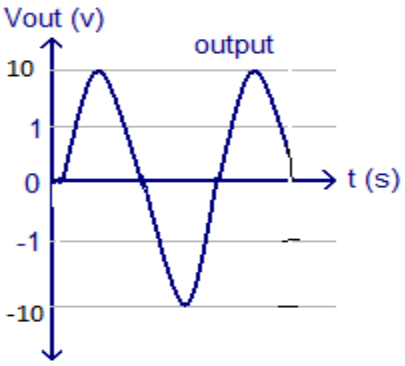



Input and Output wave forms for op-amp Non-Inverting amplifier (Gain11)

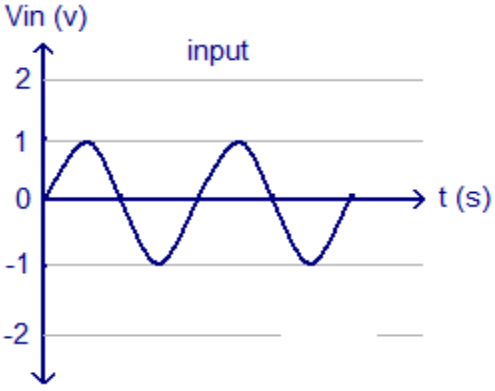
Av=Vo/ Vin

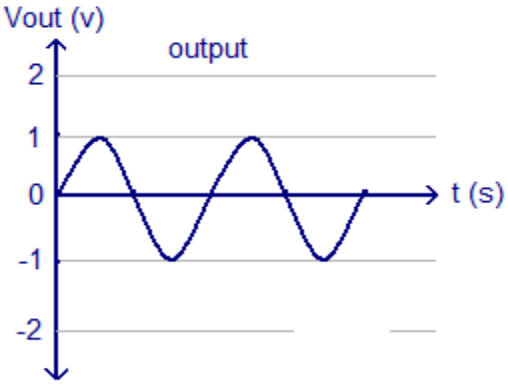



Input and Output wave forms for op-amp voltage follower (Unity Gain Amplifier)

Av=Vo/ Vin




**RESULT:**

Studied the operation of the basic applications of op-amp and Gain of the Inverting amplifier, Non-Inverting amplifier and Voltage follower were determined.

Gain of the Inverting amplifier=…….

Gain of the Non-Inverting amplifier=……..

Gain of the Voltage follower=……..

**POST LAB QUESTIONS:**

1. What is input bias current?
2. Why do we use $R_{comp}$ resistor?
3. What is thermal drift?
4. Why is IC741 op-amp not used for high frequency applications?
5. What is unity gain circuit?
6. Which amplifier acts as a Subtractor?
7. Draw the circuit diagram of 3 input adder.
8. Draw an op- amp circuit whose output $V_o$ is $V_1 + V_2 - V_3 - V_4$.

# Experiment 2

# Applications of Op-Amp

(Adder,Subtractor, Integrator and Differentiator Op-Amp)

**AIM :-**

1. To design a summer circuit using op-Amp.
2. To design a subtractor circuit using op-amp.
3. Design adifferentiatortodifferentiateaninputsignalwith fmax= 1 kHz.
4. Design an integrator circuit to properly process input waveform upto 1KHz.

**APPARATUS REQUIRED**:

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- μA741C | 1 |
| Resistor-1KΩ | 3 |
| Resistor-1.5KΩ | 2 |
| Resistor-15KΩ | 1 |
| Resistor-10k | 4 |
| Resistor-150Ω | 1 |
| Resistor-100k | 1 |
| Capacitor-0.01uf | 1 |
| Capacitor-0.1uf | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:-**

**SUMMER:-**

Op-Amp may be used to design a circuit whose output is the sum of several input signals such as circuit is called a summing amplifier or summer. We can obtain either inverting or non-inverting summer.

The circuit diagrams showsatwoinputinvertingsummingamplifier.Ithastwo input voltages $V_1$and $V_2$, two input resistors $R_1$, R2and a feedback resistor $R_f$.

Assuming that op-amp is in ideal condition s and input bias current is assumed to be zero, there is no voltage drop across the resistor $R_{comp}$ and hence the non inverting input terminal is at ground potential.

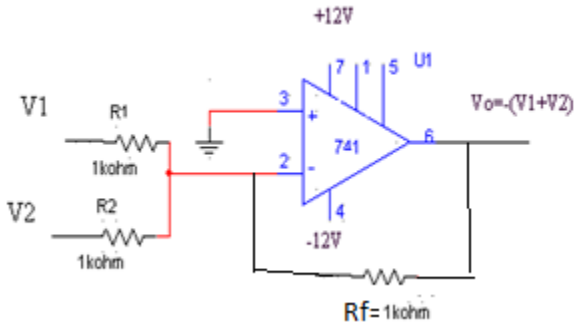
By taking nodal equations:

$V_1/R_1+V_2/R_2+V_0/R_f=0$

$V_0=-[(R_f/R_1)\ V_1+(R_f/R_2)\ V_2]$

And here $R_1=R_2=R_f=1K\Omega$

$V_0=-(V_1+V_2)$




Thus output is inverted sum ofinput.

**SUBTRACTOR:-**

Abasicdifferentialamplifiercanbeusedasasubtractor.Ithastwoinput signals V1and V2and two inputresistances R1andR2 and afeedbackresistor$R_f$.The input signals scaled to the desired values by selecting appropriate values for the external resistors.

From the figure, the output voltage ofthe differential amplifier with a gain of'1' is

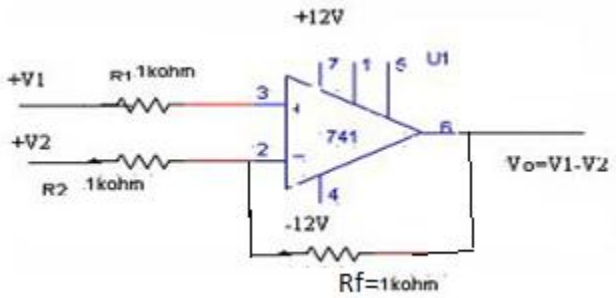
$V_0=-R/R_f(V_2-V1)$

$V_0=V_1-V_2$.

Also $R_1=R_2=R_f=1K\Omega$.

Thus,theoutputvoltage$V_0$is equaltothevoltage$V_1$appliedtothenoninverting terminal minus voltage $V_2$applied toinverting terminal.

Hence the circuit is sub tractor.



**INTEGRATOR:-**A circuit in which the output voltage is the integration of the input voltage is called an integrator**.**

$$V_o = -\frac{1}{R_1 C_f} \int V_{in}\, dt$$

In the practical integrator to reduce the error voltage at the output, a resistor $R_F$ is connected across the feedback capacitor $C_F$. Thus, $R_F$ limits the low-frequency gain and hence minimizes the variations in the output voltage.

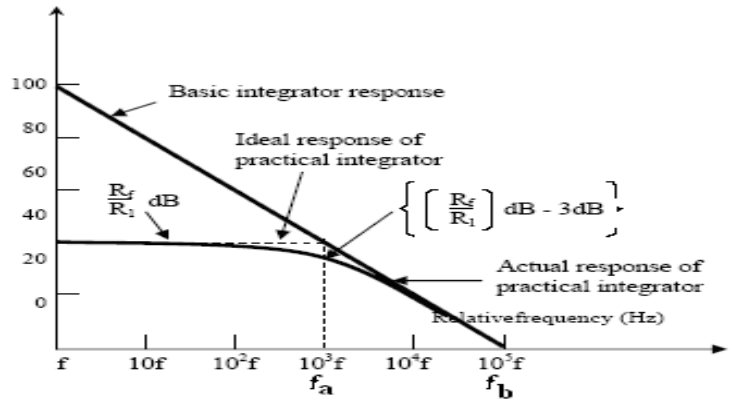



**Fig 2.1 Frequency Response of Integrator**

The frequency response of the integrator is shown in the fig. 2.1. $f_b$ is the frequency at which the gain is 0 dB and is given by $f_b = 1/2R_1C_f$.

In this fig. there is some relative operating frequency, and for frequencies from f to $f_a$ the gain $R_F/R_1$ is constant. However, after $f_a$ the gain decreases at a rate of 20 dB/decade.

In other words, between $f_a$ and $f_b$ the circuit of fig. 2.1 acts as an integrator.

The gain limiting frequency $f_a$ is given by

$f_a = 1/2\pi\, R_fC_f$.

Normally $f_a < f_b$. From the above equation, we can calculate $R_f$ by assuming $f_a$ & $C_f$.

This is very important frequency. It tells us where the useful integration range starts.

If $f_{in} < f_a$ - circuit acts like a simple inverting amplifier and no integration results,

If $f_{in} = f_a$ - integration takes place with only 50% accuracy results,

If $f_{in} = 10f_a$ - integration takes place with 99% accuracy results.

In the circuit diagram of Integrator, the values are calculated by assuming $f_a$ as 50Hz. Hence the input frequency is to be taken as 500Hz to get 99% accuracy results.

Integrator has wide applications in

1. Analog computers used for solving differential equations in simulation arrangements.
2. A/D Converters
3. Signal wave shaping
4. Function Generators.

**DESIGN**:-

The frequency responses of the practical and ideal integrator are shown in the above figure. For both circuits, the crossover frequency $f_b$, at which the gain is 0 dB, is given by:

$$f_b=1/2\pi R_1C_f$$

The 3 dB cutoff frequency $f_a$ of the practical circuit is given by:

$$f_a=1/2\pi R_fC_f$$

Choose $f_b=10f_a$

$C_f=0.01\mu f$

As, $f_b=1/2\pi R_1C_f$ =1KHz

So, R1=15.9K≈16KΩ

Now ,$f_a= f_b/10$=100Hz

$f_a=1/2\pi R_fC_f$

Rf=160KΩ

& Rcomp= R1 ‖ Rf≈15KΩ

**DIFFERENTIATOR:-**

As the name suggests, the circuit performs the mathematical operation of differentiation, i.e. the output voltage is the derivative of the input voltage.

$$V_o = - R_f C_1 \frac{dV_{in}}{dt}$$

Both the stability and the high-frequency noise problems can be corrected by the addition of two components: $R_1$ and $C_f$, as shown in the circuit diagram. This circuit is a practical differentiator. The input signal will be differentiated properly if the time period T of the input signal is larger than or equal to $R_fC_1$. That is, T>= $R_fC_1$

Differentiator can be designed by implementing the following steps.

1. Select $f_a$ equal to the highest frequency of the input signal to be differentiated.

Then, assuming a value of $C_1<1\ \mu F$, calculate the value of $R_f$

2. Calculate the values of $R_1$and $C_f$ so that $R_1C_1=R_fC_f$.

Differentiator has wide applications in

1. Monostable Multivibrator
2. Signal wave shaping
3. Function Generators.

**DESIGN:-**

$\mathbf{f}_b$=fmax=1kHz

$f_b=1/2\pi R_1C_f$

Assume $C_1$=0.1μf

So, Rf=1.5KΩ

$f_a=1/2\pi R_1C_1=10\mathbf{f}_b$

$f_a$=10Khz

R1=159Ω≈150Ω

Now , $R_1C_1= R_fC_f$

$C_f=R_1C_1/= R_f$

$C_f$=0.01μf

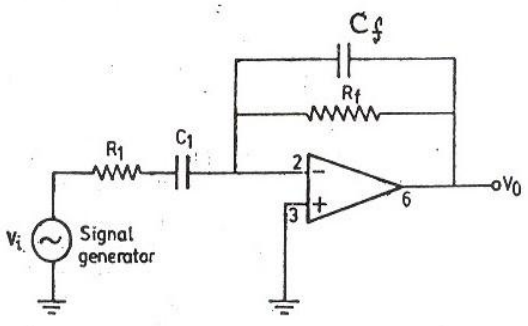



Fig 1 differentiator

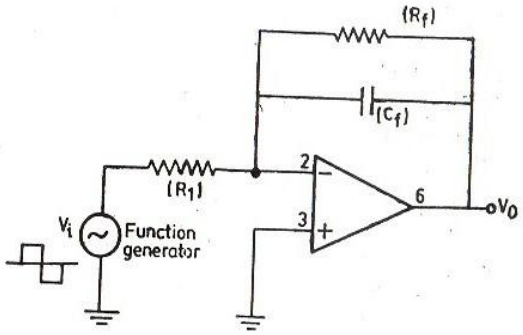



Fig. 2 integrator

**PROCEDURE:-**

**SUMMER:-**

a. Connect the Circuit shown in above figure and Apply 1V(p-p)& 0.5V(p-p) and 1 Khz sine wave signals as input .
b. Observe the output wave

**SUBTRACTOR:-**

a. Connect the Circuit shown in above figure and Apply 1V(p-p)& 0.5V(p-p) and 1 Kz sine wave signals as input
**b.** Observe the output wave.

**INTEGRATOR:-**

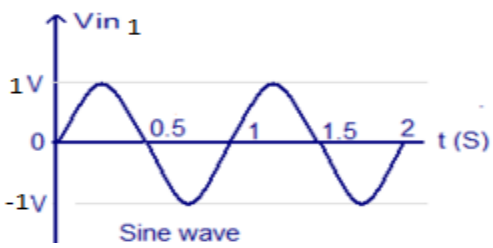
a. Connect the components/equipment as shown in the circuit diagram.
b. Switch ON the power supply.
c. Apply sine wave at the input terminals of the circuit using function Generator.
d. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
e. Observe the output of the circuit on the CRO which is a cosine wave ($90_o$ phase shifted from the sine wave input) and note down the position, the amplitude and the time period of $V_{in}$ & $V_o$.
f. Now apply the square wave as input signal.
g. Observe the output of the circuit on the CRO which is a triangular wave and note down the position, the amplitude and the time period of $V_{in}$ & $V_o$.
h. Plot the output voltages corresponding to sine and square wave inputs.

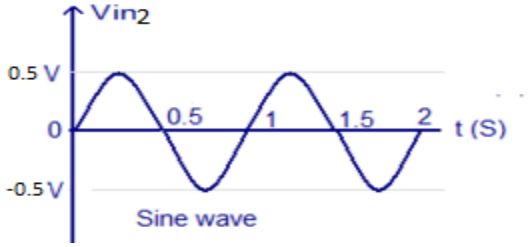
**DIFFERENTIATOR:-**

a. Connect the components/equipment as shown in the circuit diagram.
b. Switch ON the power supply.
c. Apply sine wave at the input terminals of the circuit using function Generator.
d. Connect channel-1 of CRO at the input terminals and channel-2 at the output terminals.
e. Observe the output of the circuit on the CRO which is a cosine wave ($90_o$ phase shifted from the sine wave input) and note down the position, the amplitude and the time period of $V_{in}$ & $V_o$.
f. Now apply the square wave as input signal.
g. Observe the output of the circuit on the CRO which is a spike wave and note down the position, the amplitude and the time period of $V_{in}$ & $V_o$.
h. Plot the output voltages corresponding to sine and square wave inputs.

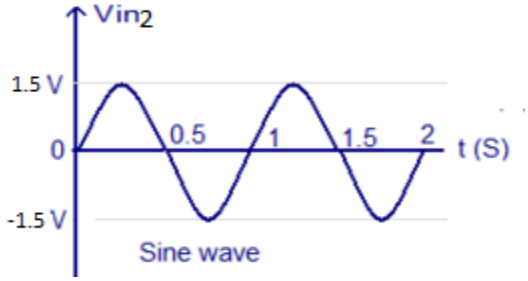
**EXPECTED GRAPHS:-**

**SUMMER:- input**

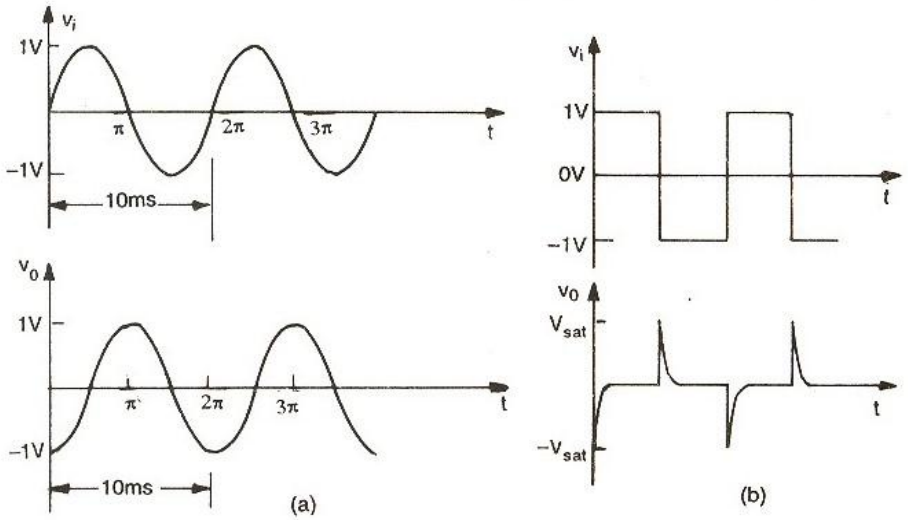


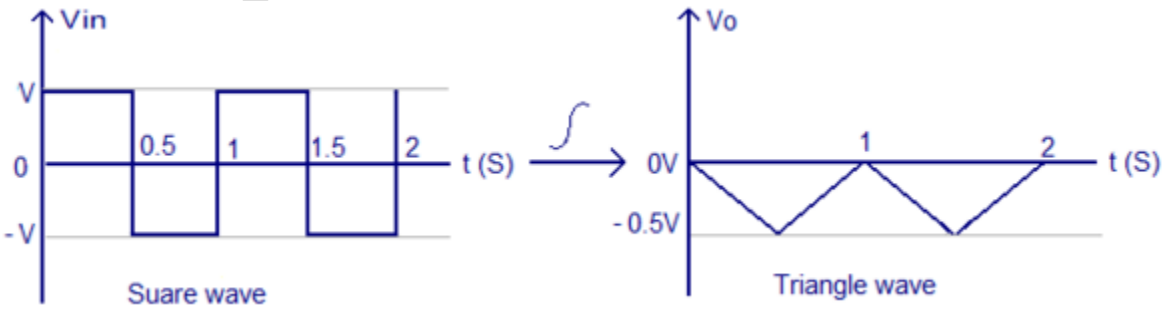

**Output:-**

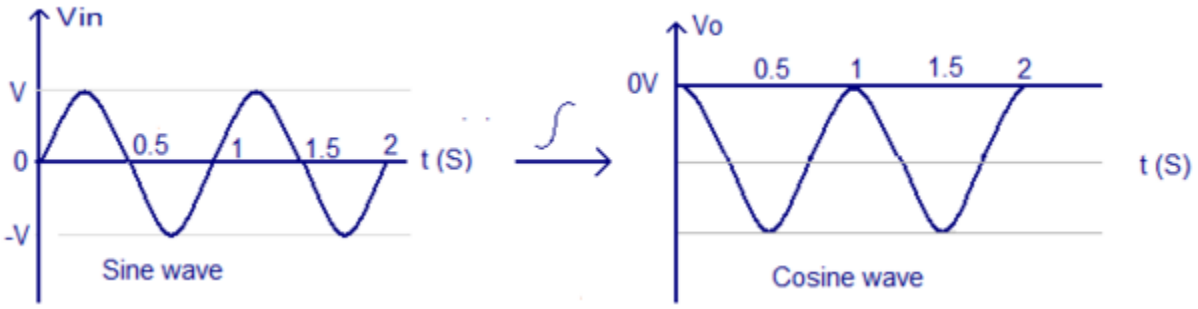



**DIFFERENTIATOR:--**




**INTEGRATOR:-**






**RESULT:-**

**POST LAB QUESTIONS:-**

1. What is an Integrator?
2. Draw the circuit of the Integrator using op-amp IC741.
3. Write down the expression for $V_o$ of an Integrator.
4. Draw the frequency response of the Integrator and explain.
5. Draw the output waveform of the Integrator when the input is a Square wave.
6. What is the purpose behind the connection of Rf in the feedback path of Integrator?
7. What are the applications of Integrator?
8. Why $R_{comp}$ is used in both Integrator and Differentiator circuits?
9. What is a Differentiator?
10. Draw the circuit of the Differentiator using op-amp IC741.
11. Write down the expression for $V_o$ of a Differentiator.
12. Draw the output waveform of the Differentiator when the input is a Sine wave.
13. Why R1 and Cf are connected in the circuit of the Differentiator?
14. What are the applications of Differentiator?

# Experiment 3

# ACTIVE FILTERS

**AIM:-** To design a first order low pass ,high pass filter at a cut off frequency of 1Khz with a pass band gain at 2.
To design a first order Butterworth narrow band passfilter at a cut off frequency of 10Khz with Q=10.

**APPARATUS REQUIRED**:

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- µA741C | 1 |
| Resistor-15KΩ | 1 |
| Resistor-1KΩ | 1 |
| Resistor-10kΩ | 3 |
| Resistor-100Ω | 1 |
| Capacitor-0.01uf,1nf | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THOERY:-**
Filters are classified as follows: Based on components used in the circuit

1. Active filters – Use active elements like transistor or op-amp(provides gain) in addition to passive elements
2. Passive filters – Use only passive elements like resistors, capacitors and inductors, hence no gain here.

Based on frequency range

1. Low pass filter(LPF) – Allows low frequencies
2. High pass filter(HPF) – Allows high frequencies
3. Band pass filter(BPF) – Allows band of frequencies
4. Band reject filter(BRF) – Rejects band of frequencies

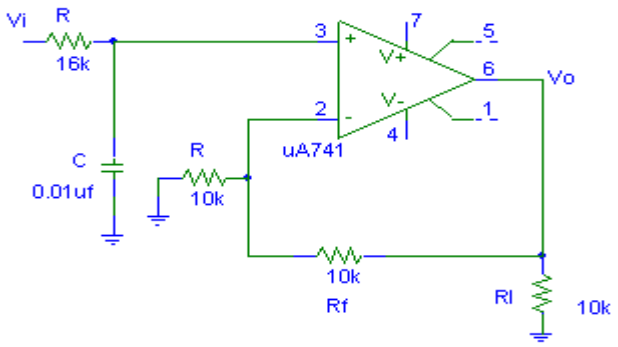
All pass filter – Allows all frequencies but with a phase shift Active Filter is often a frequency – selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. These Active Filters are most extensively used in the field of communications and signal processing. They are employed in one form or another in almost all sophisticated electronic systems such as Radio, Television, Telephone, Radar, Space Satellites, and Bio-Medical Equipment. Active Filters employ transistors or Op – Amps in addition to that of resistors and capacitors. Active filters have the following advantages over passive filters. (1) Flexible gain and frequency adjustment. (2) No loading problem (because of high input impedance and low output impedance) and (3) Active filters are more economical than passive filters.

**DESIGN:-**

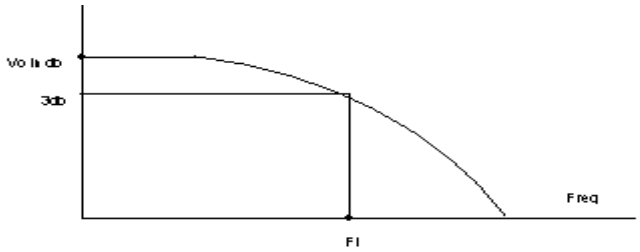
**FIRST ORDER LOW PASS FILTER:-**

Cut off frequency is given as
Fc=1khz
Select C=0.01uf
R= 1/2pifcC=16K
Pass band gain is given as 2
A=1+Rf/R1
2= 1+Rf/R1
⇨ Rf=R1=10K

**CIRCUIT DIAGRAM:-**



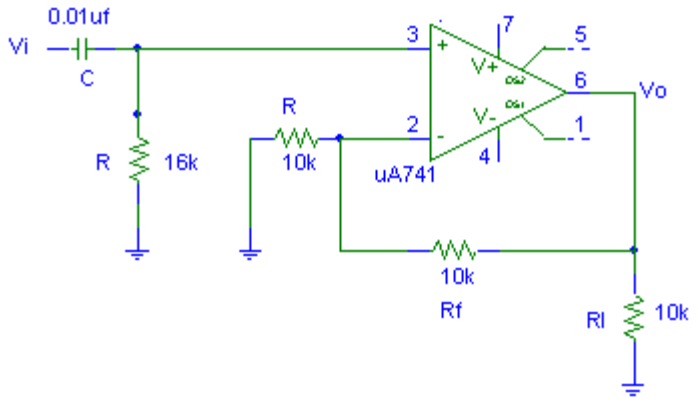

**EXPECTED GRAPH:-**



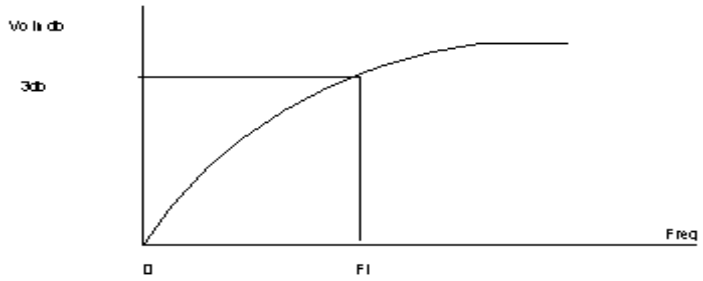

**FIRST ORDER HIGH PASS FILTER :-**

Cut off frequency is given as
Fc=1khz
Select C=0.01uf
R= 1/2pifcC=16K
Pass band gain is given as 2
A=1+Rf/R1
2= 1+Rf/R1
⇨ Rf=R1=10K

**CIRCUIT DIAGRAM:-**




**EXPECTED GRAPH:-**




**NARROW BAND PASS FILTER:-**

Pass Band gain is given as

A=10

Fc=10Khz

Q=10

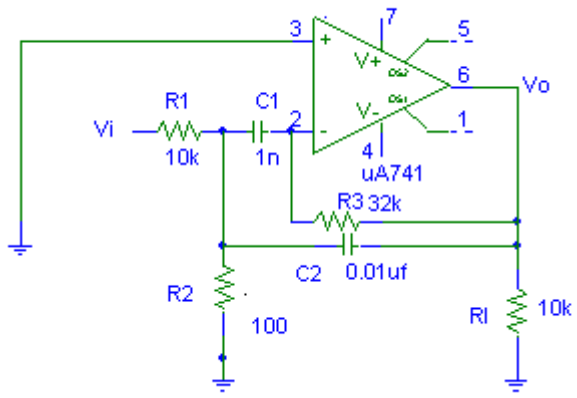
C=0.01uf

R1=q/2pifc.C.A =1.6k

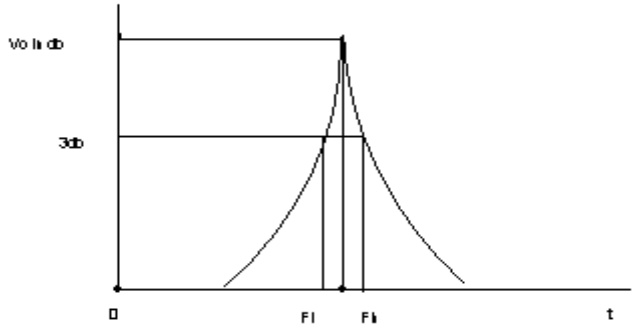
R2=Q/2pi.fc.C.($2Q^2$-A) =100Ω

R3=Q/2pifc.C =32KΩ

**CIRCUIT DIAGRAM:-**




**EXPECTED GRAPH:-**




**PROCEDURE:-**

1. Connect the circuit as shown in figure.
2. Adjust $V_{in}$=4v(P-P) & keep it constant thought-out the experiment .
3. Vary the input frequency from 20Hz to 20KHz & Note down peak to peak voltage across Rl using CRO.
4. Plot variations of voltage gain v/s frequency on semilog graph & find 3 db frequency.

**Observations& Calculations:**

| Frequency(Hz) | Input Voltage(V) | Output Voltage(V) | Gain |
|---|---|---|---|
| 100 | | | |
| 500 | | | |
| 800 | | | |
| 1K | | | |
| 1.5K | | | |
| 2K | | | |
| 8K | | | |
| 15K | | | |
| 20K | | | |
| 30K | | | |
| 50K | | | |

**RESULT:-** The filters are designed to give specifications & their frequency response is plotted as shown.

**POST LAB QUESTIONS:-**

1. How filters are classified? Give one example for each classification.
2. What is an active filter and why it is called so?
3. How an active filter differs from a passive filter?
4. What are the advantages of active filters over passive filters?
5. Draw the circuit diagrams of active filters LPF and HPF.
6. Draw the frequency response of all filters (LPF, HPF, BPF, BRF and All-pass).
7. What is the gain roll off rate for a $1^{st}$ order and $2^{nd}$ order filter?
8. What is the formula for cut-off frequency?
9. What is a 3 dB frequency and why it is called so?
10. What are the other names for 3 dB frequency?

# Experiment 4

## (Schmitt trigger, Triangular wave generator & Square wave generator using Op-amp)

### A. SCHMITT TRIGGER

**AIM:-**Determine the threshold voltage $V_{UT}$& $V_{LT}$& Draw the output waveforms of a Schmitt trigger circuit with Vin(p-p)=6V,R1=1kΩ,R2=4KΩ, VCC/VEE= ±12V(or ±15V).

**APPARATUS REQUIRED:-**

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- μA741C | 1 |
| Resistor-3.9KΩ,1KΩ,100Ω,10kΩ | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:-**

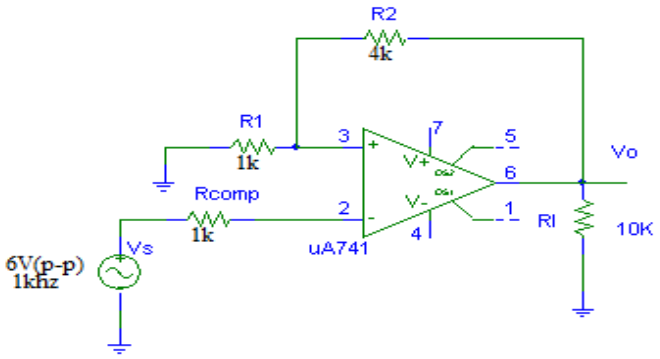
Circuit shows an inverting comparator with positive feedback. This circuit converts an irregular shaped waveform to square wave or pulse. This circuit is known as Schmitt trigger or Regenerative comparator or Squaring circuit. The input voltage Vin triggers the output Vo every time it exceeds certain voltage levels called Upper threshold voltage, VUT and Lower threshold voltage, VLT. The hysteresis width is the difference between these two threshold voltages i.e. VUT – VLT. These threshold voltages are calculated as follows.

$V_{UT} = (R_1/R_1+R_2)\ V_{sat}$ when $V_o = V_{sat}$

$V_{LT} = (R_1/R_1+R_2)\ (-V_{sat})$ when $V_o = -V_{sat}$

The output of Schmitt trigger is a square wave when the input is sine wave or triangular wave, where as if the input is a saw tooth wave then the output is a pulse wave.

**CIRCUIT DIAGRAM:-**




**PROCEDURE:-**

1. Connections are made as per the circuit.
2. Apply input sine wave of $V_{pp}$=6v, freq=1khz. Observe its corresponding output square wave & note down its time period.
3. Observe +Ve hystersis curve & note down the values for $V_{UT}$& $V_{LT}$&hence Vh finally compare the +Ve theoretical &Practical values.

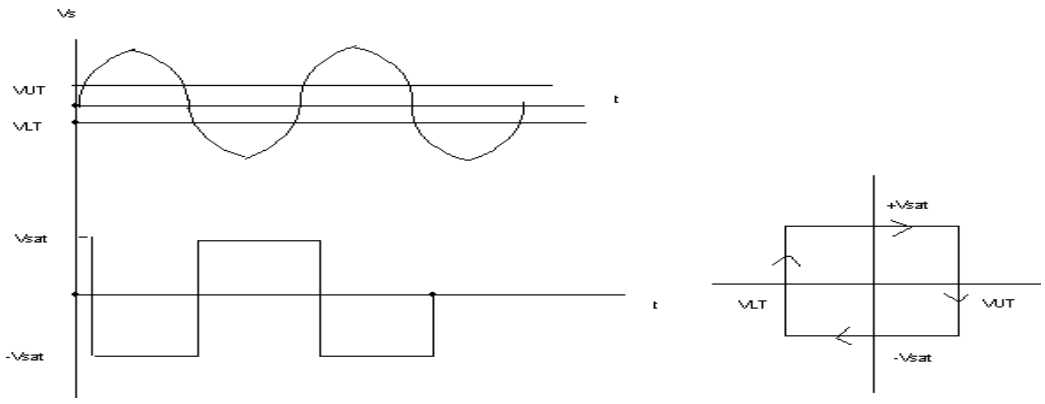
**Calculations:-**

±VCC=±12V, +Vsat=±90% of Vcc=±10.8V,
$V_{UT}$=R1/(R1+R2)(+Vsat)= 2.2V
$V_{LT}$=R1/(R1+R2)(-Vsat)= -2.2V
Hysterises voltage Vh=4.4VV
Rcomp=R1||R2=800Ω

**Observations:-**

$V_{UT}$=
$V_{LT}$=
Vh=
Time period of the wave=

**EXPECTED GRAPHS:-**



**RESULT:-**

## B. TRIANGULAR WAVW GENARATOR

**AIM:** - Design a Triangular wave generator of 1Khz using ua741 op-amp with Vpp=5V, VCC=+15v, VEE= -15V.Determine the threshold voltage $V_{UT}$& $V_{LT}$& Draw the output waveforms.

**APPARATUS REQUIRED:-**

**Components:**

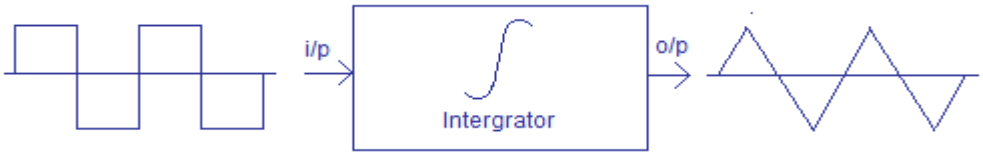
| Name | Quantity |
|---|---|
| Op-amp- µA741C | 1 |
| Resistor-56KΩ,139KΩ,10kΩ | 1 |
| Capacitors-0.01µf | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY :-**

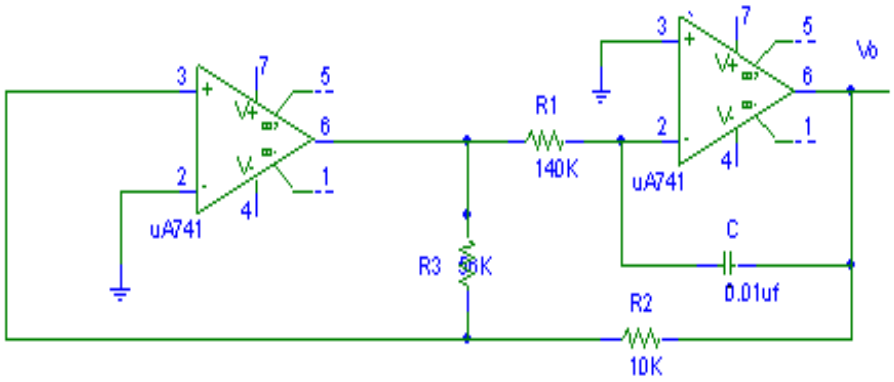
Triangular wave is a periodic, non-sinusoidal waveform with a triangular shape. People often get confused between triangle and sawtooth waves. The most important feature of a triangular wave is that it has equal rise and fall times while asawtooth wave has un-equal rise and fall times. The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc. There are many methods for generating triangular waves but here we focus on method using opamps. This circuit is based on the fact that a square wave on integration gives a triangular wave.




Generating triangular wave from a square wave

The circuit uses an opamp based square wave generator for producing the square wave and an op-amp based integrator for integrating the square wave. The circuit diagram is shown in the figure below.

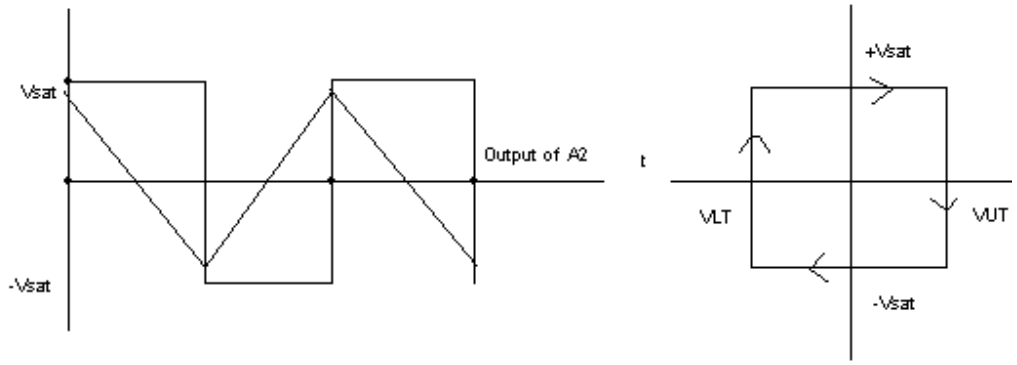
**CIRCUIT DIAGRAM:-**




**PROCEDURE:-**

1. Connection are made as per the circuit diagram.
2. Observe the Square waveform (a). The output of A1 & Triangular waveform(b). the output A2.
3. Observe the hysterisis curve & Note down the values for the $V_{UT}$&$V_{LT}$& hence $V_H$(Hysterisis curve).

**EXPECTED GRAPHS**




**DESIGN:-**

fo=1Khz, Vpp2V,VCC=-VEE=15V,±Vsat=14V
R2=10KΩ,C1=0.01uf
V pp=2R2/R3.Vsat
R3= 2R2.Vsat/Vpp=56K(use 100K plot)
fo= R3/(4R1C1R2).
=>R1=140KΩ

**OBSERVATIONS:-**

+Vsat= -Vsat=
+Vramp= -Vramp=
$V_{UT}$= $V_{LT}$=
Vh=
Time period of the wave=

## C. SQUARE WAVE GEANERATOR

**AIM:-**Design a Square wave generator of 1Khz using ua741 op-amp with Vpp=5V, VCC=+15v, VEE= -15V.$V_{UT=}V_{LT=5V}$
Draw the output waveforms & waveforms across the Capacitor.

**APPARATUS REQUIRED:-**

**Components:**

| Name | Quantity |
|---|---|
| Op-amp- µA741C | 1 |
| Resistor-1.5KΩ,1KΩ,100Ω | 1 |
| Resistor-10kΩ | 3 |
| Capacitor-0.1µf | 2 |

**Equipment:**

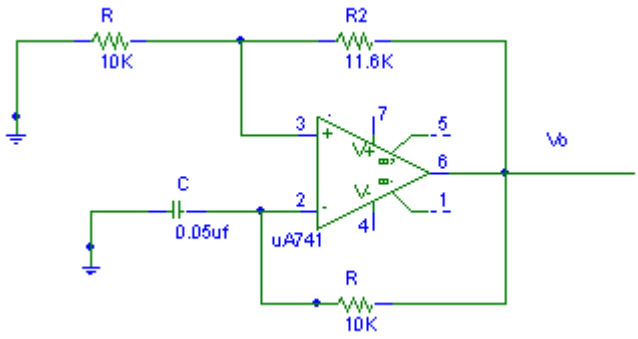
| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Dual trace CRO | 0-200MHz | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:-**

Square waves belonging to a wide range of frequencies and duty cycle can be generated using the uA741 opamp. The circuit diagram of a typical square wave oscillator using uA741 is shown in the figure below.

In the circuit diagram capacitor C1 and potentiometer R1 forms the timing part. Resistors R2 and R3 forms a voltage divider network which supplies a fixed fraction of the output voltage into the non-inverting pin of the opamp as a reference voltage.

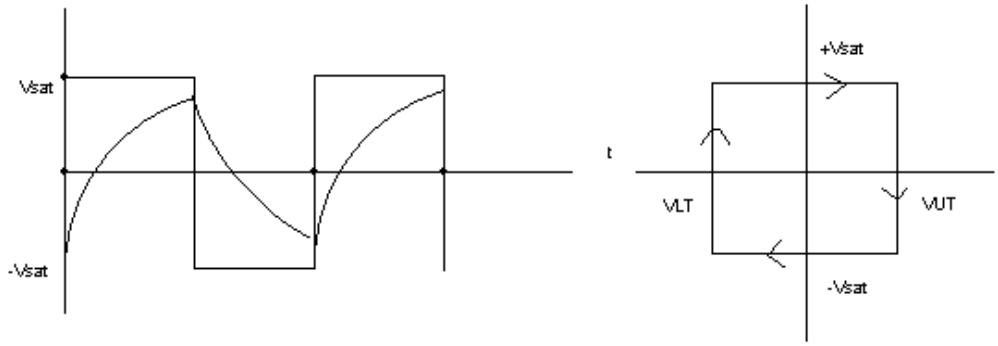
**CIRCUIT DIAGRAM:-**




**PROCEDURE:-**

1. Connection are made as per the circuit diagram.
2 .Observe the output waveform across pin np.6 of op-amp& Across capacitor &note down the amplitude & time period.
3. Observe the hysterisis curve & Note down the values for the $V_{UT}$&$V_{LT}$& hence $V_H$(Hysterisis curve).

**EXPECTED GRAPHS:-**




**DESIGN:-**

R1=10KΩ, R2=1.16KR1=11.6KΩ=12KΩ
F0=1/2RC
=>R=1/2f0C=10KΩ
**$V_{UT}$:-**
$V_{UT}$=(R1/R1+R2)V sat=5V
⇨ V sat=(R1+R2/R1)$V_{UT}$=11V
**$V_{LT}$:-**
$V_{LT}$=(R1/R1+R2)-V sat=5V
⇨ V sat=-(R1+R2/R1)$V_{LT==}$11V.
**Observations:-**
+Vsat=
-Vsat=
$V_{UT}$=

$V_{LT}$=
Vh=
Time period of the wave=

**RESULT:-** A Schmitt trigger circuit, Triangular wave generator, square wave generator are designed & their waveforms are studied.

**POST LAB QUESTIONS:-**

1. Which is type of comparator called Schmitt trigger using IC741?
2. What is the output wave of Schmitt trigger if the input is sine wave?
3. What type of waveform is obtained when triangular or ramp waveforms are applied to Schmitt trigger circuit?
4. Explain how a square wave is obtained at the output of timer when sine wave input is given?
5. What is the Threshold voltage?
6. How do you calculate the theoretical values of $V_{UT}$ and $V_{LT}$ in the case of IC741 ?
7. What do you mean by monostable multivibrator?
8. What is an astable multivibrator?
9. Disadvantage of Monostable Multivibrators?
10. Application of Monostable Multivibrators?

# Experiment -5

# NE-555 TIMER APPLICATIONS
# A. ASTABLE MULTIVIBRATOR

**AIM:-**TO design an Astable multivibrator using 555 timer & to generate q square wave of 75% duty cycle & amplitude 5V ,freq=1Khz

**APPARATUS**:-

**Components:**

| Name | Quantity |
|---|---|
| IC 555 | 1 |
| Resistor-7.2KΩ,3.2KΩ | 1 |
| Capacitor-0.01µf | 1 |
| Capacitor-0.1µf | 2 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:-**

A astable multivibrator, often called a free-running multivibrator, is a rectangular-wavegenerating circuit. Unlike the monostable multivibrator this circuit does not require any external triggering to change the state of the output, hence the name free-running. However, the time during which the output is either high or low is determined by the two resistors and a capacitor, which are externally connected to the 555 timer.

**Astable operation:** Initially when output is high, capacitor C starts charging toward Vcc through RA and RB. However as soon as voltage across the capacitor equals 2/3 Vcc, comparator 1 triggers the flip-flop, and the output switches low. Now capacitor C stars discharging through RB and transistor Q1 . When the voltage across C equals 1/3 Vcc, comparator 2's output triggers the flip-flop, and the output goes high. Then the cycle repeats. The output voltage and capacitor voltage are shown IN GRAPHS.

As shown in this figure, the capacitor is periodically charged and discharged between 2/3 Vcc and 1/3 Vcc, respectively. The time during which the capacitor charge from 1/3 Vcc to 2/3 Vcc is equal to the time the output is high and is given by

$t_c = 0.69(R_A + R_B) C$ ……..(a)

Where RA and RB are in ohms and C is in farads.

Similarly, the time during which the capacitor discharges from 2/3Vcc to 1/3Vcc is equal to the time the output is low and is given by

$t_d = 0.69(R_A) C$ ……..(b)

Thus the total period of output waveform is

$T = t_c + t_d = 0.69(R_A + 2R_B) C$ ……..(c)

Frequency of Oscillation is

$f_o = 1/T = . 1.45 / (R_A + 2R_B) C$ ----------(d)

Duty Cycle:- The duty cycle is the ratio of the time tc during which the output is high to the total time period T. It is generally expressed as a percentage.

% duty cycle =( tc /T)× 100

= ((RA + RB) /(RA + 2RB))X100 …….(e)

**DESIGN:-**

Given duty cycle=75%

ferq=1Khz

f=1.45/(RA+2RB)C

Assume C=0.1uf

=>RA+2RB=1.45/0.1uf*1K=1.45KΩ

RB/(RA+2RB)=25/100

=>4RB=RA+2RB=>RA=2RB

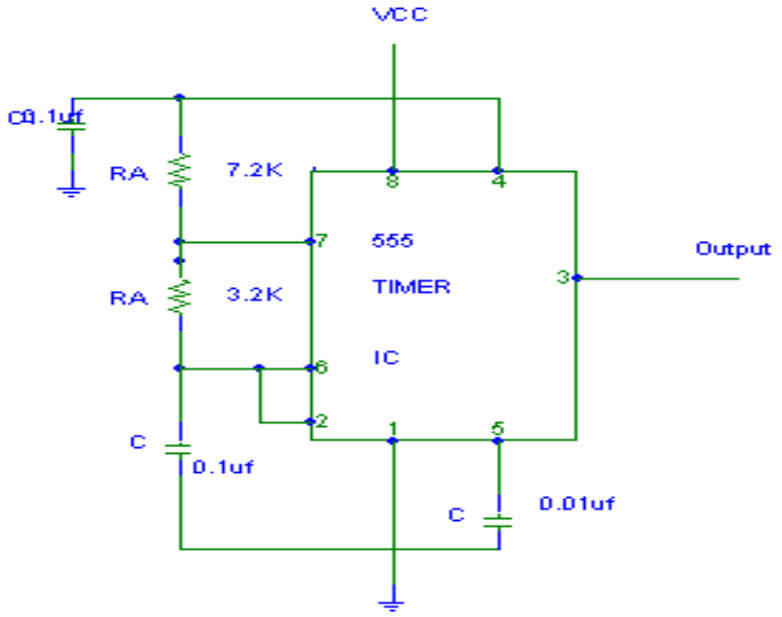
but RA+2RB=1.45kΩ

⇨ 4RB=14.5KΩ

⇨ RB=36.25K=3.7KΩ

⇨ RA=14.5K-2RB=7.2KΩ

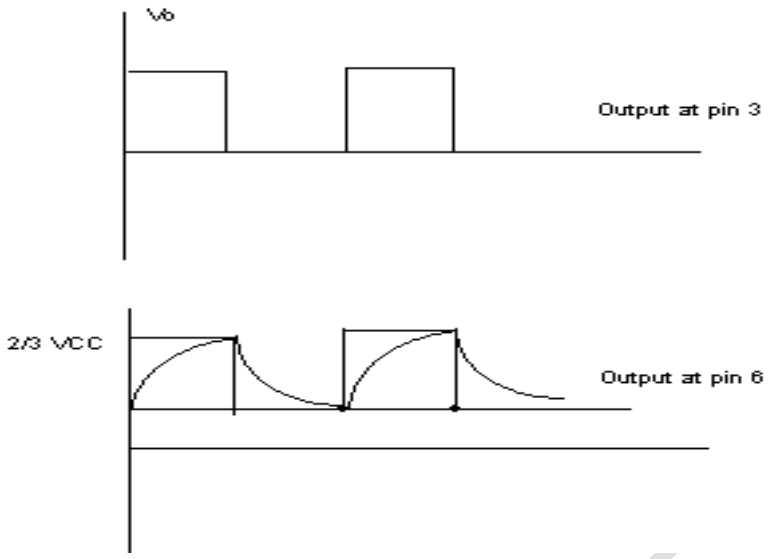
**CIRCUIT DIAGRAM:-**




**PROCEDURE:-**

1. Connections are made as per the circuit diagram.
2. Observe the output wave form (a). pin3 & Compare it with theoretical value.
3. Also observe the waveform (a) pin6 (across c) & check that amplitude should by 2/3 VCC.

**EXPECTED WAVE FORMS:-**




**OBSERVATIONS:-**

$T_{low}$=0.7*0.5ms
$T_{high}$=1.9*0.5ms=0.95ms
$T=T_{low}+T_{high}$=1.3ms
Duty cycle=0.35ms/1.3,ms=26.9%

**RESULT:-** An Astable multivibrator is designed using 555 timer which generates a square wave.

## B. MONOSTABLE MULTIVIBRATOR USING 555 TIMER

**AIM:-** **(a)**TO design a monostable multivibrator using 555 timer to generate a pulse width of 1ms & amplitude of 5V for each trigger input.
**(b).** Draw the waveforms at A,B,C,D,E.

**APPRARATUS**:-

**Components:**

| Name | Quantity |
|---|---|
| IC 555 | 1 |
| DA9A Diode | 1 |
| Resistor-KΩ,10KΩ | 1 |
| Capacitor-0.01μf | 1 |

| | |
|---|---|
| Capacitor-0.1µf | 1 |
| Capacitor-10uf | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**THEORY:-**

A monostable multivibrator, often called a one-shot multivibrator, is a Pulse generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby state the output of the circuit is approximately zero or at logic-low level. When an external trigger pulse is applied, the output is forced to go high (≅ Vcc). The time the output remains high is determined by the external RC network connected to the timer. AT the end of the timing interval, the output automatically reverts back to its logic-low stable state. The output remains low until the trigger pulse is again applied. Then the cycle repeats. The monostable circuit has only one stable state (output low), hence the name monostable. Normally, the output of the monostable multivibrator is low.

**Monostable operation**: Initially when output is low, that is , the circuit is in a stable state, transistor Q1 is on and the capacitor C is shorted out of the ground. However, upon application of a negative trigger pulse to pin 2, transistor Q1 is turned off, which releases the short circuit across the external capacitor C and drives the output high. The capacitor C now starts charging up toward Vcc through RA. However, when the voltage across the capacitor equals 2/3 Vcc, comparator 1's output switches from low to high, which in turn drives the output to its low state via the output of the flip-flop. At the same time, the output of the flip-flop turns transistor Q1 ON, and hence capacitor C rapidly discharges through the transistor. The output of the monostable remains low until a trigger pulse is again applied. Then the cycle reprats. Fig.(c) shows the trigger input, output voltage, and capacitor voltage waveform. As shown here, the pulse width of the trigger input must be smaller than the expected pulse width of the output waveform. Also the trigger pulse must be a negative-going input signal with amplitude larger than 1/3 Vcc. The time duration that the output remains high is given by,

tp = 1.1RAC seconds

**DESIGN:-**

Given tp=1ms choose C=0.1uf

$tp=1.1R_AC$

⇨ $R_A=1*10^{-3}/(1.1*0.1*10^{-6})=10K\Omega$

Wave shaping network for a good differentiation

Select R1C1<<tp

Let R1C1/tp=0.01

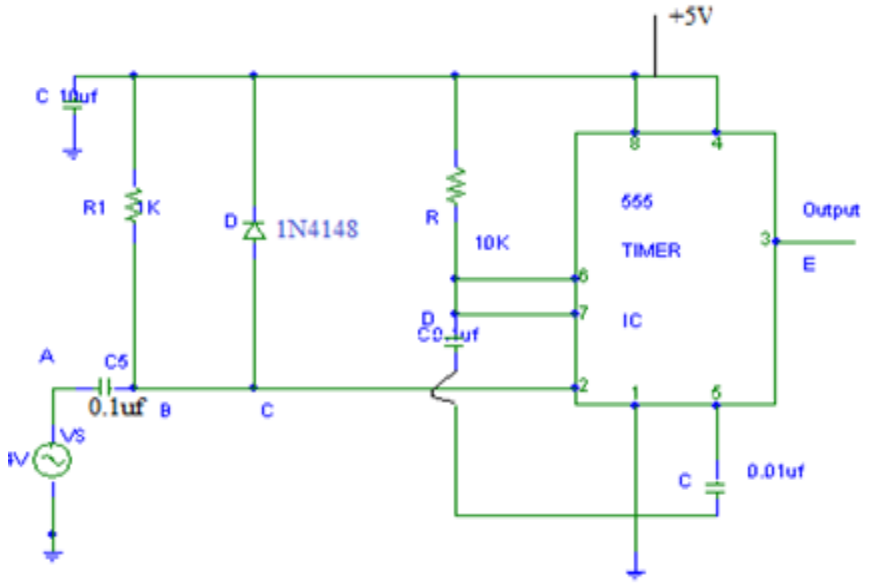
Choose C1=0.01uf

⇨ $R1=(0.01*10^{-3})/(0.01*10^{-6})=1K\Omega$

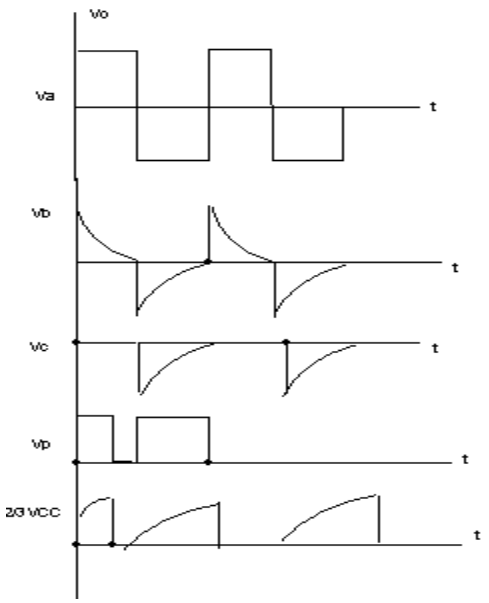
Designed component values are

$C=0.1uf, C1=0.01uf, R1=1K\Omega, R_A=10K\Omega$

**CIRCUIT DIAGRAM:-**




**EXPECTED GRAPHS :-**




**PROCEDURE:-**

1. Connections are made as per the circuit diagram]
2. Apply input trigger voltage at pin2 of 555 timer IC
3. Note down the waveforms at A,B,C,D,&E.
4. Measure the pulse width of the output waveforms at pin 3.

**RESULT:-** A Monostable multivibrator is designed using 555 timer which generates a pulse width.

**POST LAB QUESTIONS:-**

1. What is the other name for monostable multivibrator (MSMV)?
2. When MSMV is in stable state, what is the output level?
3. Why trigger is required in the case of MSMV?
4. Which type of trigger pulse is required for MSMV?
5. What is the formula for the output pulse width of MSMV?
6. How long MSMV stays in unstable state?
7. Explain the functional block diagram of a 555 timer
8. Explain the function of reset.
9. What are the modes of operation of timer?
10. What is the expression of time delay of a monostable multivibrator?
11. Discuss some applications of timer in monostable mode.
12. Define duty cycle
13. Give methods of obtaining symmetrical waveform.
14. . How is an monostable multivibrator connected into a pulse position modulator
15. How Schmitt trigger circuit is constructed using 555 timer
16. Draw the pin diagram of 555 timer

# Experiment -6

## VOLTAGE REGULATORUSING IC 723

AIM:-Toplot the regulation characteristics ofthegiven IC LM 723.

**APPARATUS::-**

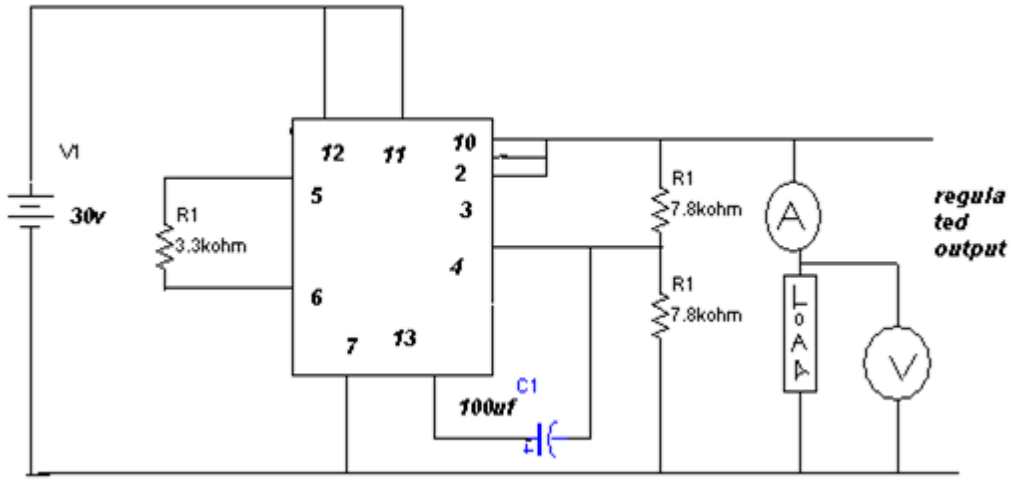
**Components:**

| Name | Quantity |
|---|---|
| IC LM 723 | 1 |
| DA9A Diode | 1 |
| Resistor-7.8KΩ ,3.9KΩ | 1 |
| Capacitor-100µF | 1 |
| DRB | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**CIRCUIT DIAGRAM:**




**THEORY:**

A voltage regulator is a circuit that supplies constant voltage regard less of changes in load currents. Except for the switching regulators, all other types of regulatorsarecalledlinearregulators.ICLM723isgeneralpurposeregulator.The input voltage of this 723 IC is 40V maximum. Output voltage adjustable from 2Vto30V. 150Ma output current external pass transistor. Output currents in excess of 10Ampere possible by adding external transistors.Itcan be used as either a linear or a switching regulator. The variation of DC output voltage as a function – of DC load current is called regulation.

% Regulation =[(Vnl-Vfl)/Vfl]*100

**PROCEDURE:**

**(1).LINE EGULATION**

1.Connections are made as per the circuit diagram
2.Power supply is connected to12 and 7 terminals
3.Volt meter is connected to10 and 7 terminals
4.Byincreasing the input voltage corresponding volt meter reading is noted.

**(2).LOAD REGULATION**

1. Connect the load tothe terminals 10 and GND.
2. Keep the input voltage constant atwhich line regulation is obtained
3. The maximum load value is calculated from IC ratings.
4. Now,wedecreasetheloadresistanceandnotedownthecorresponding Values Ofthe output in volt meter.
5. Plot the graph forload verses load regulation.

**OBSERVATIONS:**

**(1).LINEREGULATION**:

Vnl=

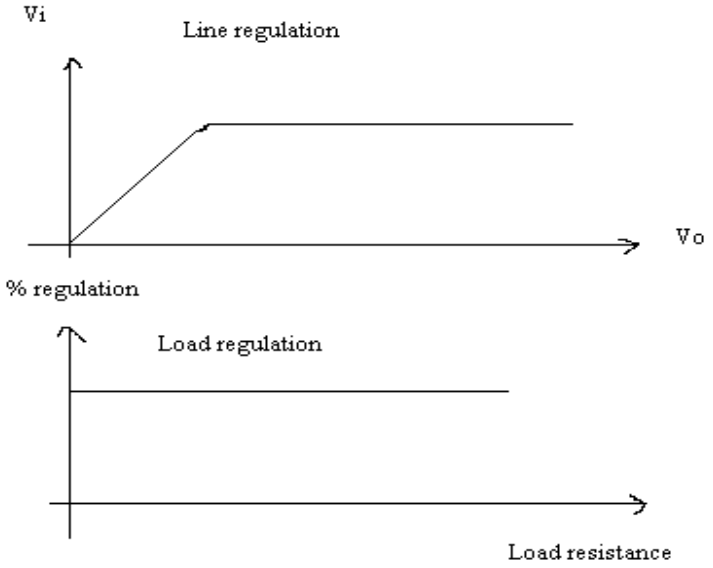
| Line voltage (V) | Outputvoltage(V) |
|---|---|
| | |

**(2).LOAD REGULATION**:

| Regulated output(V) | Load current(mA) | Load resistance(KΩ) | Load regulation |
|---|---|---|---|
| | | | |

% REGULATION=[(Vnl-Vfl)/Vfl]*100

**MODEL GRAPH:**




**PRECAUTIONS:**

1.Whiletakingthereadingsofregulatedoutputvoltageloadregulation ,keep the input voltage constant at15V.

2.Donotincrease the input voltage morethan 30 Vwhile taking thereadingforno load condition?

**RESULT:**



# Experiment 7

## Three Terminal Voltage Regulators (7805, 7809 And 7912)

**AIM:**

To verify the operation of three terminal fixed voltage regulators 7805, 7809, 7912 and also to find out their line and load regulation.

**APPARATUS:**

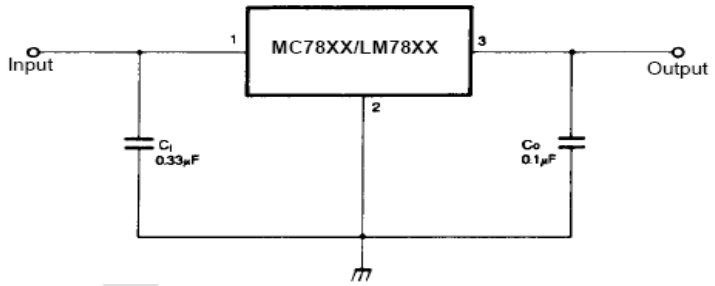
**Components:**

| Name | Quantity |
|---|---|
| IC 7805,7809,7912 | 1 |
| Capacitor-0.33uf,0.1uf | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Multimeter | | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**CIRCUIT DIAGRAM:**




**THEORY:**

Three terminal voltage regulators have three terminals which are unregulated input ($V_{in}$), regulated output ($V_o$) and common or a ground terminal. These regulators do not require any feedback connections.

**Positive voltage regulators:**

78xx is the series of three terminal positive voltage regulators in which xx indicate the output voltage rating of the IC.

**7805:**

This is a three terminal regulator which gives a regulated output of +5V fixed. The maximum unregulated input voltage which can be applied to 7805 is 35V.

**7809:**

This is also three terminal fixed regulator which gives regulated voltage of +9V.

Negative voltage regulators:

79xx is the series of negative voltage regulators which gives a fixed negative voltage as output according to the value of xx.

**7912:**

This is a negative three terminal voltage regulator which gives a output of -12V.

**Line Regulation:**

It is defined as the change in the output voltage for a given change in the input voltage. It is expressed as a percentage of output voltage or in millivolts.

$\%R_L = \Delta V_o/\Delta V_{in}$ x 100

**Load Regulation:**

It is the change in output voltage over a given range of load currents that is from full load to no load. It is usually expressed in millivolts or as a percentage of output voltage.

$\%R_{Load} = [(V_{nl}-V_{fl})/V_{nl}]$ x100

**PROCEDURE:**

1. Connect the circuit as shown in the figure.
2. Apply unregulated voltage from 7.5V to 35V and observe the output voltage.
3. Calculate the line and load regulation for the regulator.
4. Plot the graphs from the observations.
5. Repeat the same for the remaining regulators.

## Result



## Experiment-8

# IC 566 –VCO APPLICATIONS

**AIM:**

Tooperatethe NE/SE566 asVoltageControlledOscillatorandtofind the Frequenciesfor various values of$R_1$and $C_1$;

**APPARATUS:**

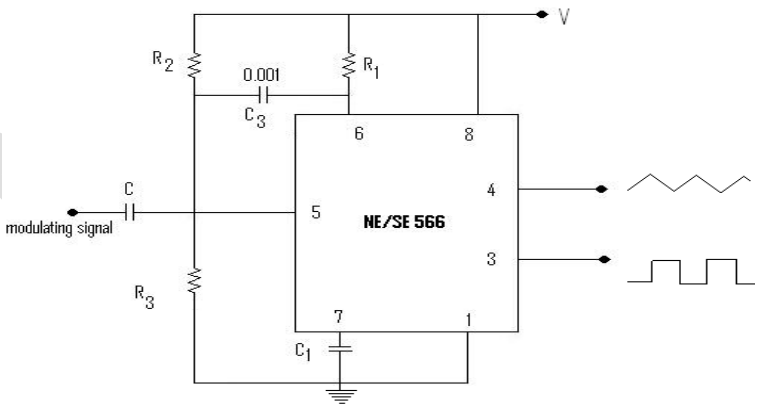
**Components:**

| Name | Quantity |
|---|---|
| IC NE/SE566 | 1 |
| DA9A Diode | 1 |
| Resistors-1KΩ,5KΩ,4KΩ,6KΩ,8KΩ | 1 |
| Capacitors- 0.001μF,0.0001μF | 1 |

**Equipment:**

| Name | Range | Quantity |
|---|---|---|
| IC Trainer board | | 1 |
| Function generator | 0-20MHz. | 1 |
| Connecting Wires& CRO Probes | | |
| Power supply | 220V,50 Hz | |

**CIRCUIT DIAGRAM:**




**THEORY:**

VoltageControlledOscillatorisalsocalledasvoltagetofrequencyconverter.Itprovidesthesimultaneous squarewaveandtriangularwaveoutput.Thefrequencyofoutputwaveisthefunctionofinput voltage,hencethenameVoltageControlledOscillator.Outputfrequencyisalsothefunctionofexternalresistor$R_1$andcapacitor$C_1$.

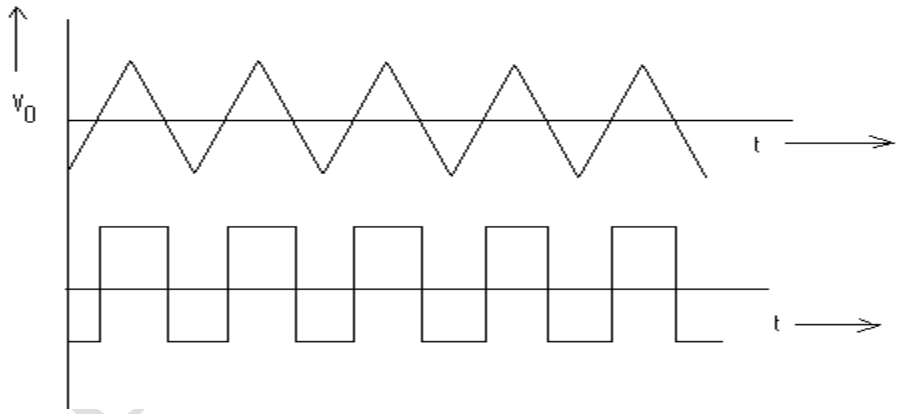
**PROCEDURE**

1.Connections are made as per the circuit diagram.
2.Measure the output voltage and frequency ofboth triangular and squares.
3.Vary the values of$R_1$and $C_1$and measure the frequency ofthe waveforms.
4.Compare the measured values with the theoretical values.

**OBSERVATIONS**

| Sl. No. | $R_1$ | $C_1$ | OutputVoltage (V) | | Theoretical frequency (KHz) $f_O = \frac{2(V - V_C)}{R_1 C_1 V}$ | Practical frequency (KHz) |
|---|---|---|---|---|---|---|
| | | | Square wave | Triangular wave | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |

**MODEL GRAPH**:




**PRECAUTIONS:**

1.Connect the wires properly.
2.Maintain proper Vcclevels.

**RESULT:**

# PART-B

# Experiment-9

## TTL, CMOS Characteristics and CMOS Logic Gates

.

**AIM:**

1. Observe and plot transfer characteristic of a TTL and CMOS inverter.
2. Measure noise margin of a TTL and CMOS inverter.
3. Measure propagation delay of a CMOS inverter
4. Test simple CMOS logic gate circuits.

**Background:**

**TTL FAMILY**

The logic family refers to the general physical realization of a logical element, such as the TTL, emittercoupled logic (ECL), or complementary metal-oxide semiconductor (CMOS) logic families. Within each logic family are one or more logic series that have distinctive characteristics, relative to other series within the same logic family. For example, in the TTL logic family, there are several logic series: the 74 standard, 74L lowpower, 74H high-speed, 74S standard Schottky, 74LS low-power Schottky series, and 74ALS advanced lowpower Schottky series. The TTL family was the most widely used logic family for several years, characterized by its relatively high speed operation. However, it has now been largely replaced by CMOS logic. The physical representation of the binary logic states in these families are high and low voltages. Assuming positive logic, in the 74LS TTL family LOW (L) voltages in the range 0 V to 0.8 V are considered to be logic 0, and HIGH (H) voltages in the range 2.0 V to 5.5 V are considered to be logic 1.

**CMOS Family**

In CMOS technology, both p-type and n-type MOSFETs are used to implement digital circuits e.g., logic gates. CMOS logic gates have the desirable properties of high noise immunity and low static power consumption. In this experiment, you will use the CD4007 chip which has 3 NMOS and 3 PMOS transistors to make simple CMOS gates and test them. The figure below shows the details of CD4007. Note that VSS (pin 7) is connected to ground and VDD (pin 14) to 5 V. This requires that, for the PMOS device (6, 13, 14), pin 14 must be treated as the source terminal, and for the NMOS device (6, 7, 8), pin 7 must be treated as the source terminal.

Parameters to look for in a logic family:

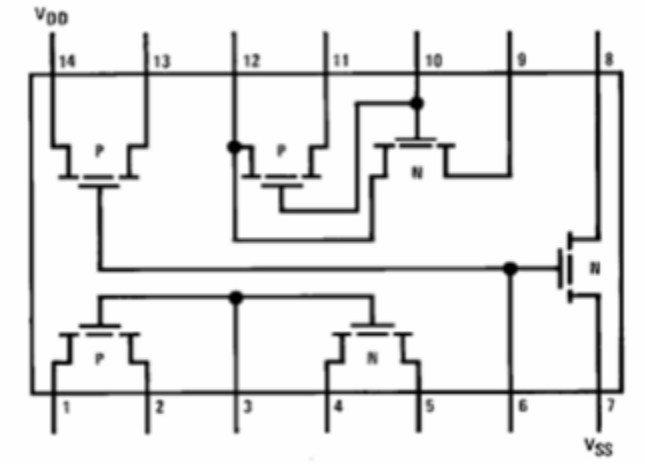
Noise Margins: The noise margins for an inverter are defined as shown in fig. 1(a).

NMHIGH = VOH - VIH, NMLOW = VIL – VOL

Propagation Delays: The propagation delays are defined as shown in fig. 1 (b).

tpLH = t2 –t1, tpHL = t4- t3, tp = (tpLH + tpHL) / 2

Rise and Fall times: The rise time and fall times are defined as shown in fig. 1 (c).



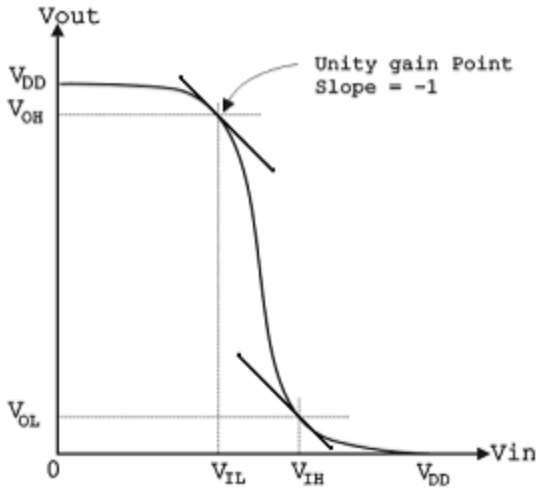




Figure 1 (a)

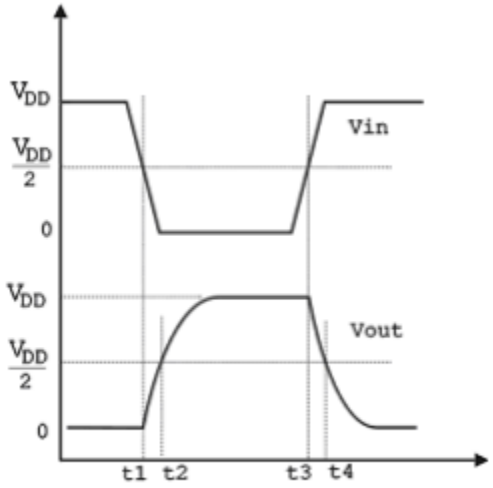



Figure 1 (b)

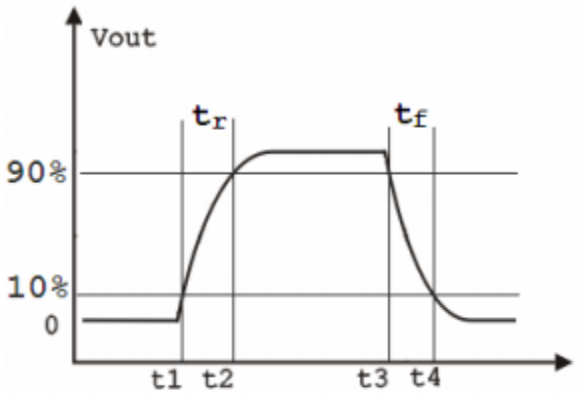



Figure 1 (c)

1. TTL Inverter gate:
   a) Vary the input voltage Vin from 0 V to 5 V in 0.1 V steps and measure the corresponding Vout with DMM.
   b) Apply 0-5 V, 2 kHz triangular wave as input at Vin. You can get this voltage range by adding an offset to the triangular wave output of the function generator. Now observe the voltage transfer curve directly on the CRO with the help of XY mode by connecting both the input and output simultaneously. Note down the values of VIL, VOL, VIH and VOH. Calculate the noise margin.
2 CMOS inverter gate:
   a) Wire the circuit shown in Fig. 2.Vary the input voltage Vin from 0 V to 5 V in 0.1 V steps and measure the corresponding Vout with a DMM
   b) Apply 0-5 V, 2 kHz triangular wave as input at Vin. You can get this voltage range by adding an offset to the triangular wave output of the function generator. Now observe the voltage transfer curve directly on the CRO with the help of XY mode by connecting both the input and output simultaneously.
   c) Apply 0-5 V, 500 kHz square wave as input. Observe the input and output waveforms on CRO. Find the rise, fall and propagation time as described in Figs. 1 (b) and (c).

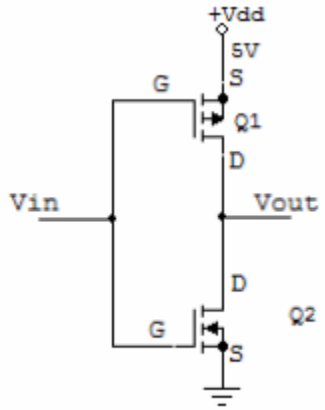



**Figure 2: CMOS inverter**

**3. CMOS NAND and NOR gates:** Connect the circuits as shown below. Measure the output voltage at Y for different combinations of input A and B, e.g., 1 and 0. Here '1' and '0' corresponds to 5 V and 0 V, respectively.

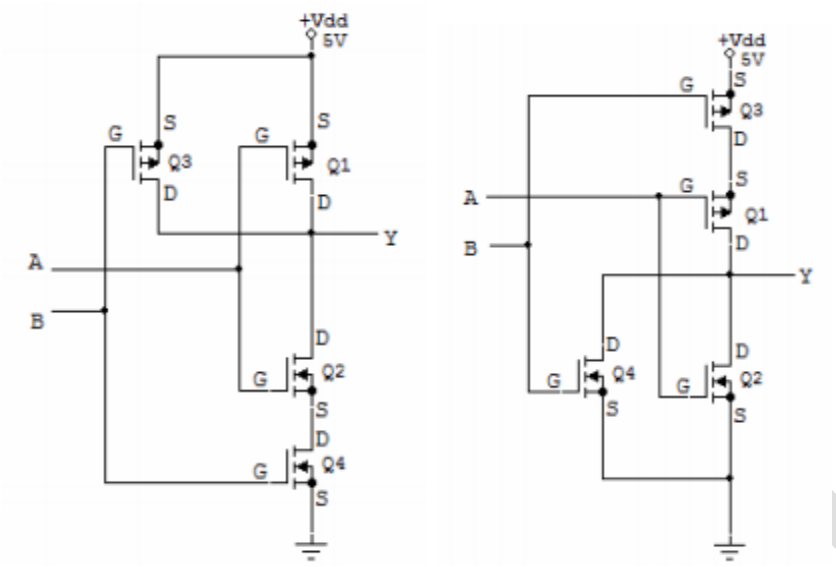



**Figure 3: CMOS NAND and NOR gates**

## RESULT:

**Post Lab work:**

1. Plot the transfer curve for the inverter using the data obtained in 1 (a) and 2 (a). Find the noisemargins.
2. Compare the noise margin, propagation delay, rise time, and fall time with the values specified in the datasheet of CD4007.

# Experiment-10
# LOGIC GATES AND CODE CONVERTERS

**AIM:-**(A). Toverify the truth table of Logic Gates.

(B). To Design and implement a 4-bit

1. Binary to Gray Code converter
2. Gray to Binary Code converter using logic gates.

## APPARATUS REQUIRED:-

1. ICs- 7400,7402,7404,7408,7432,7486.
2. Trainer Kit
3. Connecting wires

## (A). Logic Gates

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables.

AND gate:-

The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. This dot is sometimes omitted i.e. AB


| 2 Input AND gate | | |
|---|---|---|
| A | B | A.B |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

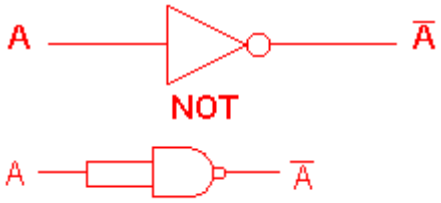
OR gate:-

The OR gate is an electronic circuit that gives a high output (1) if **one or more** of its inputs are high. A plus (+) is used to show the OR operation.

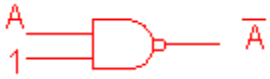

| 2 Input OR gate | | |
|---|---|---|
| A | B | A+B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

NOT gate:-

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an *inverter*. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar over the top.




| NOT gate | |
|---|---|
| A | $\overline{A}$ |
| 0 | 1 |
| 1 | 0 |



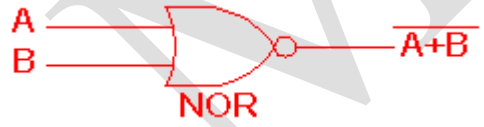

NAND gate:-

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if **any** of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.


| 2 Input NAND gate | | |
|---|---|---|
| A | B | $\overline{A.B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

NOR gate:-

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if **any** of the inputs are high.The symbol is an OR gate with a small circle on the output. The small circle represents inversion.




| 2 Input NOR gate | | |
|---|---|---|
| A | B | $\overline{A+B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

EXOR gate:-

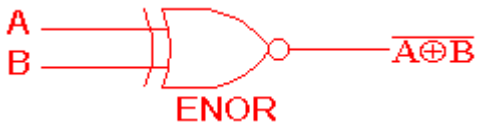
The '**Exclusive-OR**' gate is a circuit which will give a high output if **either, but not both**, of its two inputs are high. An encircled plus sign (⊕) is used to show the EOR operation


| 2 Input EXOR gate | | |
|---|---|---|
| A | B | A⊕B |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

.

EXNOR gate:-

The '**Exclusive-NOR**' gate circuit does the opposite to the EOR gate. It will give a low output if **either, but not both**, of its two inputs are high. The symbol is an EXOR gate with a small circle on the output. The small circle represents inversion.




| 2 Input EXNOR gate | | |
|---|---|---|
| A | B | $\overline{A⊕B}$ |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

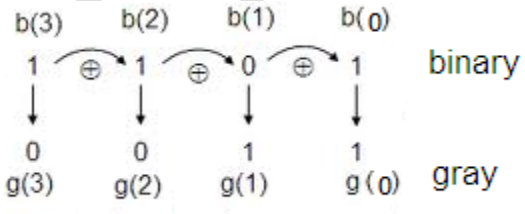
## (B). CODE CONVERTERS

**Binary code** is a way of representing the text or the data generated by the computers and other devices.In binary coding the text or the data is represented in a stream of bits of 1's and 0's .

**Gray Code** is one of the most important codes. It is a non-weighted code which belongs to a class of codes called minimum change codes. In this code while traversing from one step to another step, only one bit in the code group changes. In case of **Gray Code** two adjacent code numbers differs from each other by only one bit.

**Design:-**

1. Binary to Gray Code converter:
   The binary number and the Gray-coded number will have the same number of bits. The conversion process is shown below.

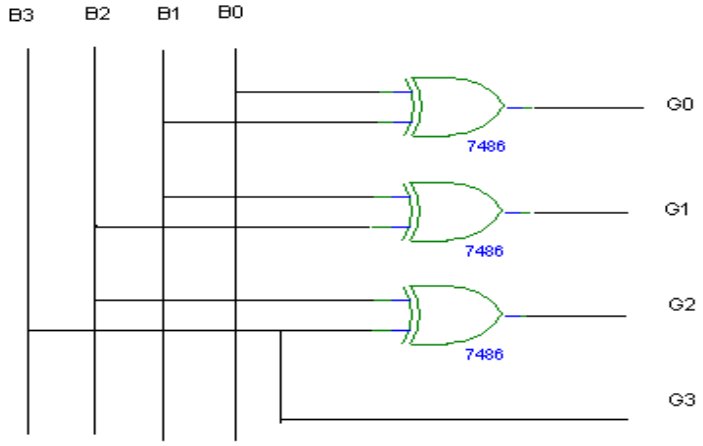


| Binary | | | | Gray | | | |
|---|---|---|---|---|---|---|---|
| B3 | B2 | B1 | B0 | G3 | G2 | G1 | G0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

(NOTE:-Find the expressions using K-map for G3, G2 ,G1, G0.)

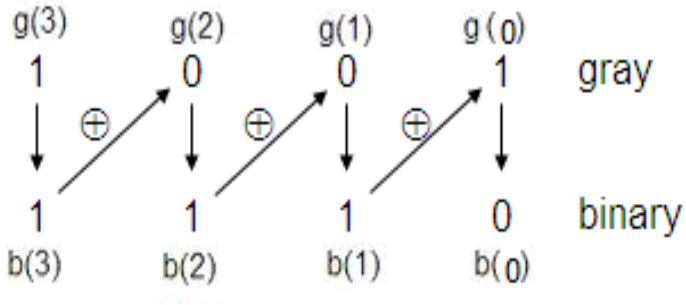
G3=B3; G2= B2B3'+B3B2'; G1= B1'B2+B2'B1; G0=B1'B0+Bo'B1

Circuit Diagram:-



2. Gray to Binary Code converter :

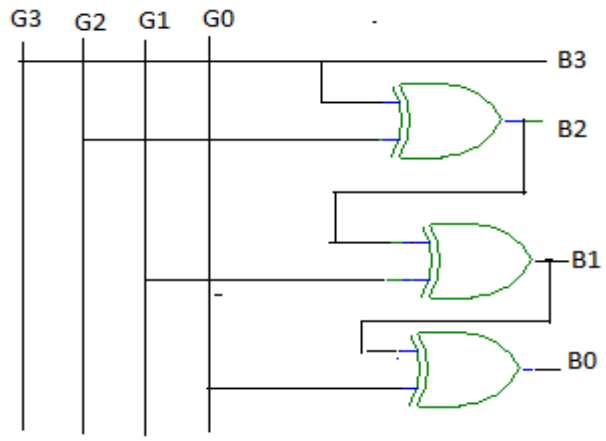
The binary number and the Gray-coded number will have the same number of bits. The conversion process is shown below.




| Gray | | | | Binary | | | |
|---|---|---|---|---|---|---|---|
| G3 | G2 | G1 | G0 | B3 | B2 | B1 | B0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |

(NOTE:-Find the expressions using K-map for G3,G2,G1,G0.)
B3=G3; B2= G2G3'+G3G2'; B1= B2 G3'+B2'G3; B0= B1G0'+B1'Go;

Circuit Diagram:-




**PROCEDURE:-**

1. The connections are made as per the circuit diagram
2. Give different inputs and observe the outputs.
3. Compare them with truth table. Repeat the same for gray to binary and BCD to Excess-3.

**RESULT: -**The truth table of logic gates has been verified and the realization of Binary to Gray And Gray to Binary code converter has been done and practically verified.

**POST LAB QUESTIONS**:

1. What are basic gates.
2. What are universal gates.
3. What two logics are considered the most versatile logic gates?
4. Which of the two input logic gate can be used to implement an inverter?
5. What are the applications of code converters?

# Experiment-11
# REALIZATION OF ADDERS AND SUBTRACTORS

**AIM:-**To design and implement Half adder , Half subtractor, Full adder & Full subtractor.

## APPARATUS REQUIRED:-

1. IC 7400-3 no.
2. Trainer Kit
3. Connecting wires.

## THEORY :-

### HALF ADDER:-

The half-adder adds two input bits and generates a carry and sum, which are the two outputs of half-adder. The input variables of a half adder are called the augend and addend bits.The output variables are the sum and carry.

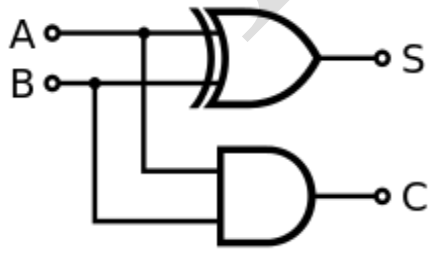
**Truth Table:-**

| A | B | Sum | Carry |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

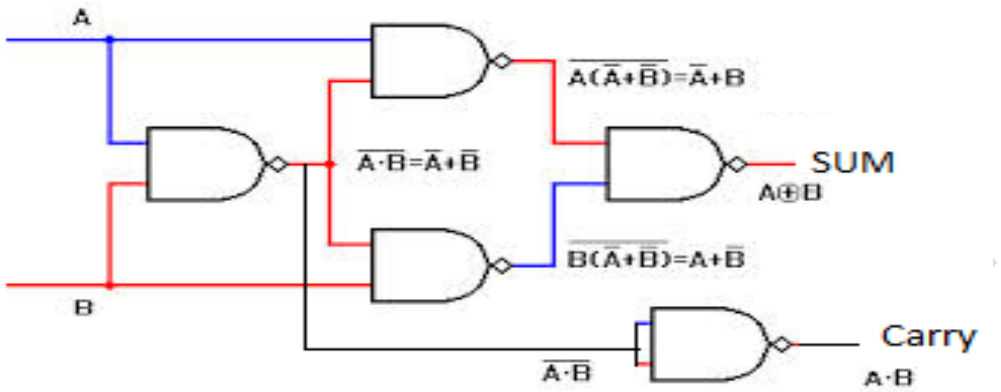
( NOTE:-Find the expressions using K-map for Sum and Carry)

Sum=A'B+AB'
Carry=AB

**Circuit Diagram**:-




**Half Adder using NAND Gates**




**Full Adder:-**

The main difference between a half-adder and a full-adder is that the full-adder has three inputs and two outputs. The first two inputs are A and B and the third input is an input carry designated as Cin**.**The output carry is designated as Cout and the normal output is designated as S.

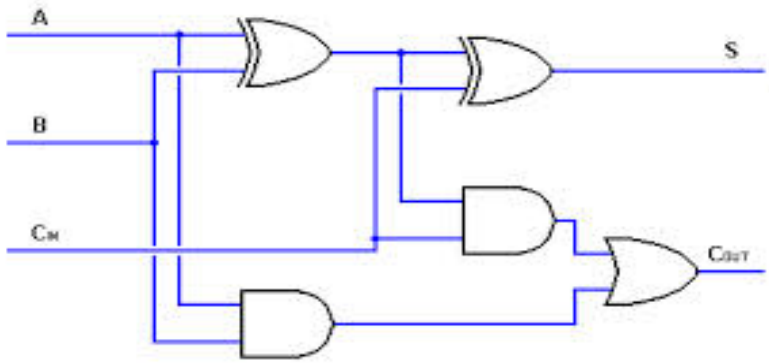
**Truth Table:-**

| A | B | Cin | Sum | Cout |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

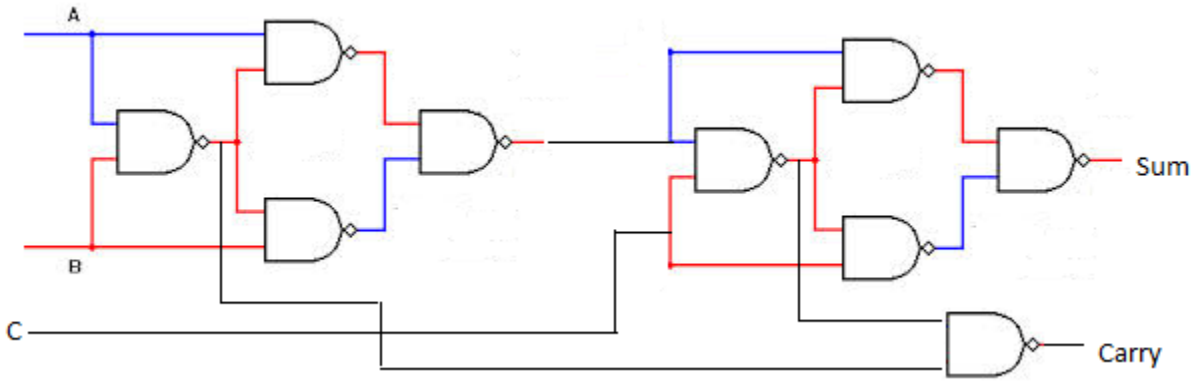
( NOTE:-Find the expressions using K-map for Sum and Carry)

Sum=A⊕B⊕Cin
Cout=AB+BCin +ACin

**Block Diagram using Gates:-**




**Full adder using NAND Gates**




**Half Subtractor :-**

The half-subtractor is a combinational circuit which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and B (borrow).

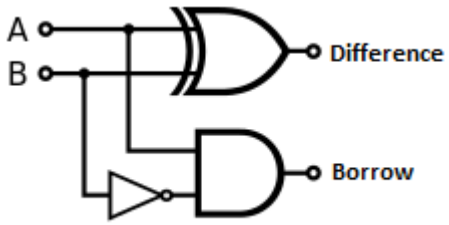
**Truth Table:-**

| A | B | D | B |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

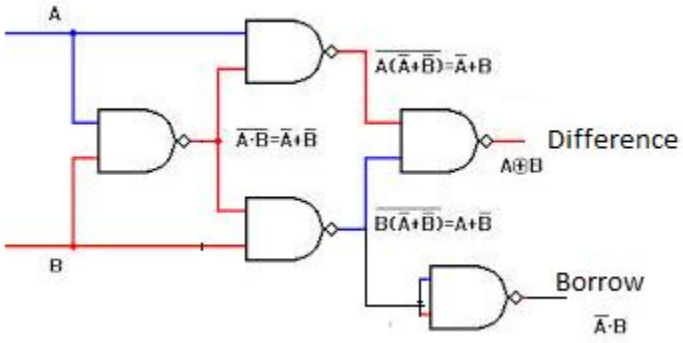
( NOTE:-Find the expressions using K-map for Difference and Borrow)

Difference =A'B+AB'
Borrow =A'B

**Circuit Diagram:-**




**Half Subtractor using NAND Gates:-**




**Full Subtractor:-**

The full-subtractor is a combinational circuit which is used to perform subtraction of three bits. It has three inputs, X (minuend) and Y(subtrahend) and Z (subtrahend) and two outputs D (difference) and B (borrow).

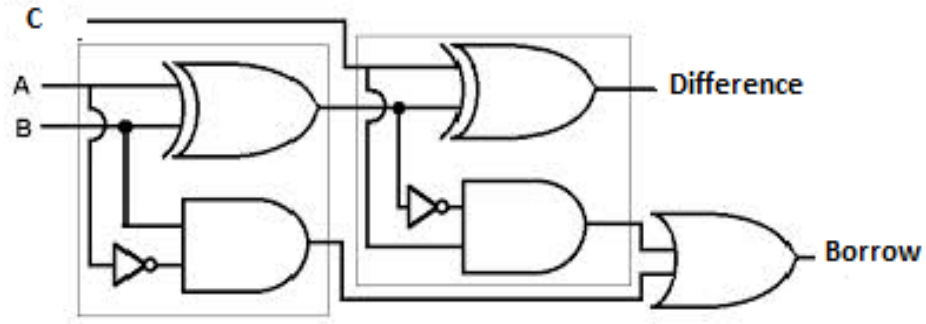
**Truth Table:-**

| A | B | C | D | B |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

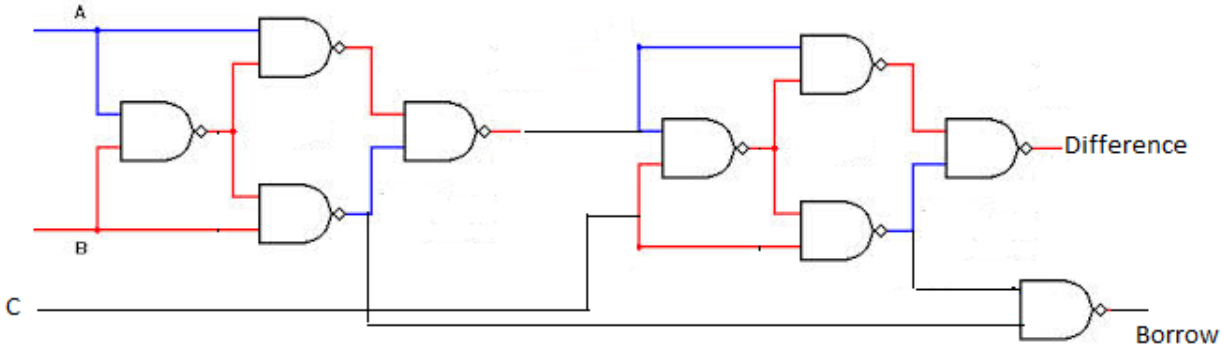
( NOTE:-Find the expressions using K-map for Difference and Borrow)

$D=A\oplus B\oplus Cin$
$B=A'B+BCin+A'Cin$

**Full Subtractor using Gates:-**




**Full subtractor using NAND Gates:-**




## PROCEDURE:-

1. Connections are made as per the circuit diagram.
2. Give different inputs and observe the outputs.
3. Compare them with truth table.

**RESULT:-**Half adder, Full adder ,Half subtractor & Full subtractors truth tables are verified.

# Experiment-12
## FLIP FLOP and CONVERSION

**AIM:-**

1. Verify the truth table of RS Latch and D Latch.
2. Verify the truth table of JK Flip Flop using Gates and IC 7476.
3. Realize D & T flip flop using JK flip flop of IC 7476.

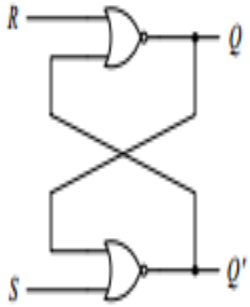
**APPARATUS REQUIRED**:-

4. ICs- 7400, 7402, 7404,7411, 7476.
5. Trainer Kit.
6. Connecting wires.

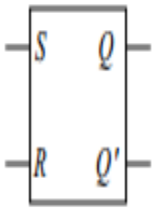
**THEORY:-**

Latches and flip-flops are the basic elements for storing information. One latch or flip-flop can store one bit of information. The main difference between latches and flip-flops is that for latches, their outputs are constantly affected by their inputs as long as the enable signal is asserted. In other words, when they are enabled, their content changes immediately when their inputs change. Flip-flops, on the other hand, have their content change only either at the rising or falling edge of the enable signal. This enable signal is usually the controlling clock signal. After the rising or falling edge of the clock, the flip-flop content remains constant even if the input changes.

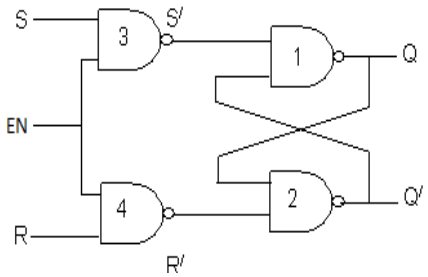
**SR LATCH :-**



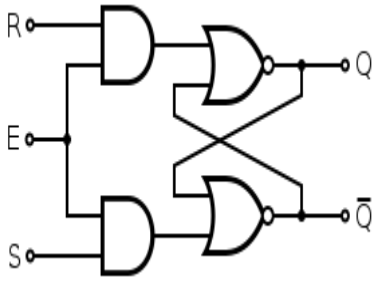

| S | R | Q | $Q_{next}$ | $Q_{next}'$ |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | x | 0 | 1 |
| 1 | 0 | x | 1 | 0 |
| 1 | 1 | x | 0 | 0 |




**SR LATCH WITH ENABLE INPUT:-**



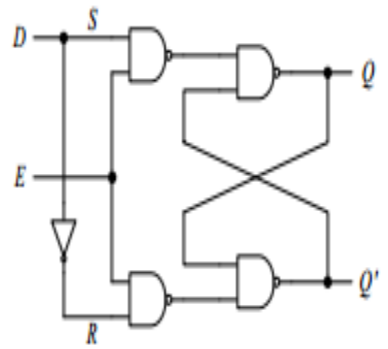

**Using NAND**




**Using NOR**

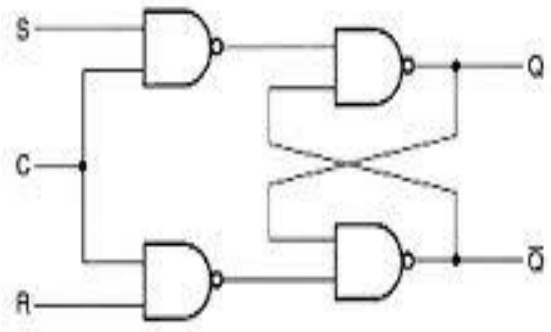
| $E$ | $S$ | $R$ | $Q$ | $Q_{next}$ | $Q_{next}'$ |
|---|---|---|---|---|---|
| 0 | × | × | 0 | 0 | 1 |
| 0 | × | × | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | × | 0 | 1 |
| 1 | 1 | 0 | × | 1 | 0 |
| 1 | 1 | 1 | × | 1 | 1 |

**D LATCH:-**




| $E$ | $D$ | $Q$ | $Q_{next}$ | $Q_{next}'$ |
|---|---|---|---|---|
| 0 | × | 0 | 0 | 1 |
| 0 | × | 1 | 1 | 0 |
| 1 | 0 | × | 0 | 1 |
| 1 | 1 | × | 1 | 0 |

**SR FLIPFLOP:-**

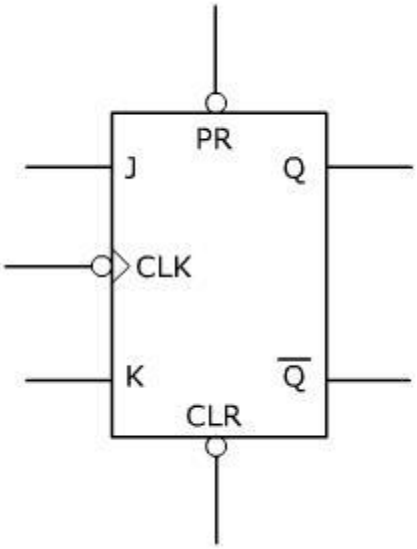


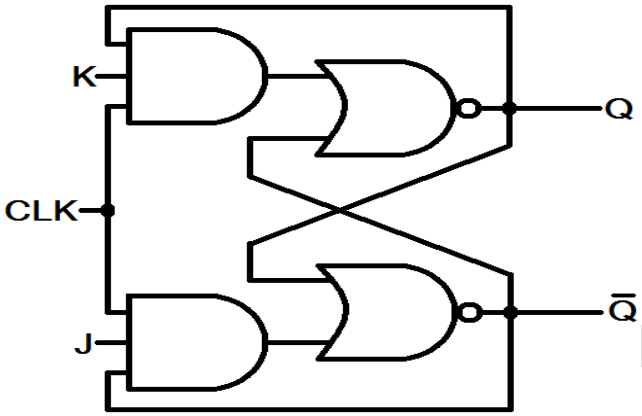

(a) Logic diagram

| C | S | R | Next state of Q |
|---|---|---|---|
| 0 | X | X | No change |
| 1 | 0 | 0 | No change |
| 1 | 0 | 1 | Q = 0; Reset state |
| 1 | 1 | 0 | Q = 1; Set state |
| 1 | 1 | 1 | Undefined |

(b) Function table

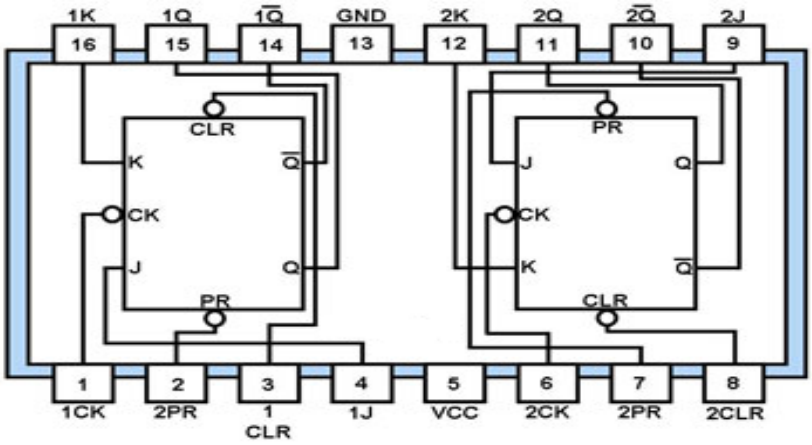
**JK FLIPFLOP:-**



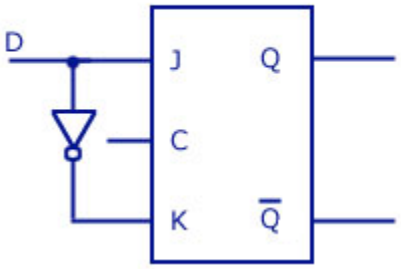

| CLOCK | J | K | $\overline{PRESET}$ | $\overline{RESET}$ | Q | $\overline{Q}$ |
|---|---|---|---|---|---|---|
| - | - | - | 0 | 1 | 1 | 0 |
| - | - | - | 1 | 0 | 0 | 1 |
| ↓ | 0 | 0 | 1 | 1 | Q | $\overline{Q}$ |
| ↓ | 1 | 0 | 1 | 1 | 1 | 0 |
| ↓ | 0 | 1 | 1 | 1 | 0 | 1 |
| ↓ | 1 | 1 | 1 | 1 | $\overline{Q}$ | Q |

**JK Flipflop using IC 7476:**



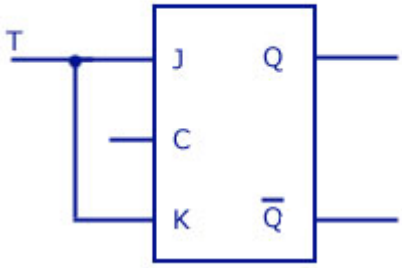
**D Flip Flop using JK Flip Flop:**

Logic Diagram




**T Flip Flop using JK Flip Flop:**

Logic Diagram




**PROCEDURE:-**

1. Connect the circuit and verify the truth tables of all flipflops.

**RESULT:-L**atches and flip flops have been verified and realization of D and T flip flop using JK Flip Flop is done successfully**.**

# Experiment-13

## SYNCHRONOUS AND ASYNCRONOUS COUNTERS

**AIM :-**

1. Design 3 bit ripple counter
2. Design & Realize mod -5 Ripple counter (CLK=1khz)
3. Design & Realize mod -5 synchronous counter (CLK=1khz) by skipping 010,100,110 states.(use JK flip flop)
4. Obtain the count sequence in IC 7490 when the output Q2 is connected to input A and pulse are applied at input B.

**APPARATUS REQUIRED:-**

7. ICs- 7476 & 7408.
8. Trainer Kit.
9. Connecting wires.

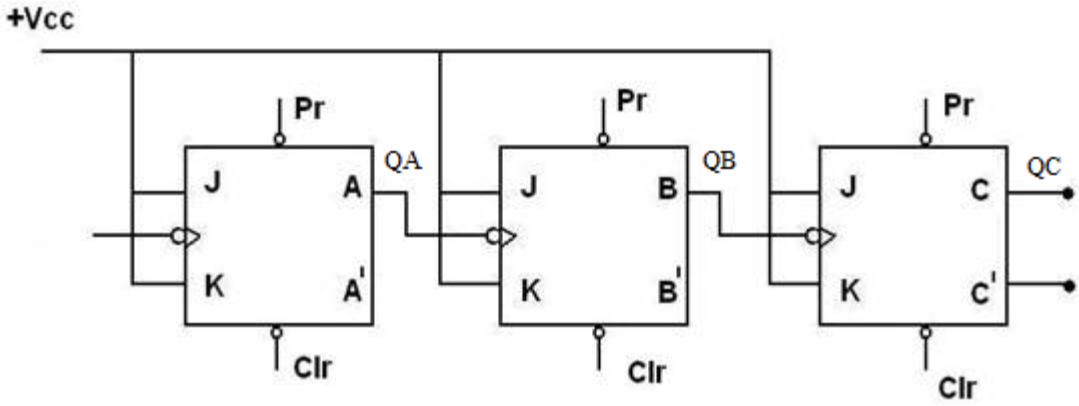
**THEORY:-**

A counter is a sequential circuit that counts in a cyclic sequence. It is essentially a register that goes through a predetermined sequence of states upon the application of input pulses. There are two types of counters – Synchronous Counter & Asynchronous Counter. In a synchronous counter, the input pulses are applied to all clock pulse inputs of all flip flops simultaneously (directly). Synchronous counter is also known as **parallel sequential circuit**. Examples of Synchronous Counters are Ring Counter and Johnson Counter (Switch Tail or Twisted Ring Counter)

In an asynchronous counter, the flip flop output transition serves as a source for triggering other flip flops. In other words, the clock pulse inputs of all flip flops, except the first, are triggered not by the incoming pulses, but rather by the transition that occurs in previous flip flop's output.. Asynchronous counter is also known as **serial sequential circuit**. Example of Asynchronous Counters are Binary Ripple Counter and Up Down Counter.Synchronous counters are faster than asynchronous counter because in synchronous counter all flip flops are clocked simultaneously.

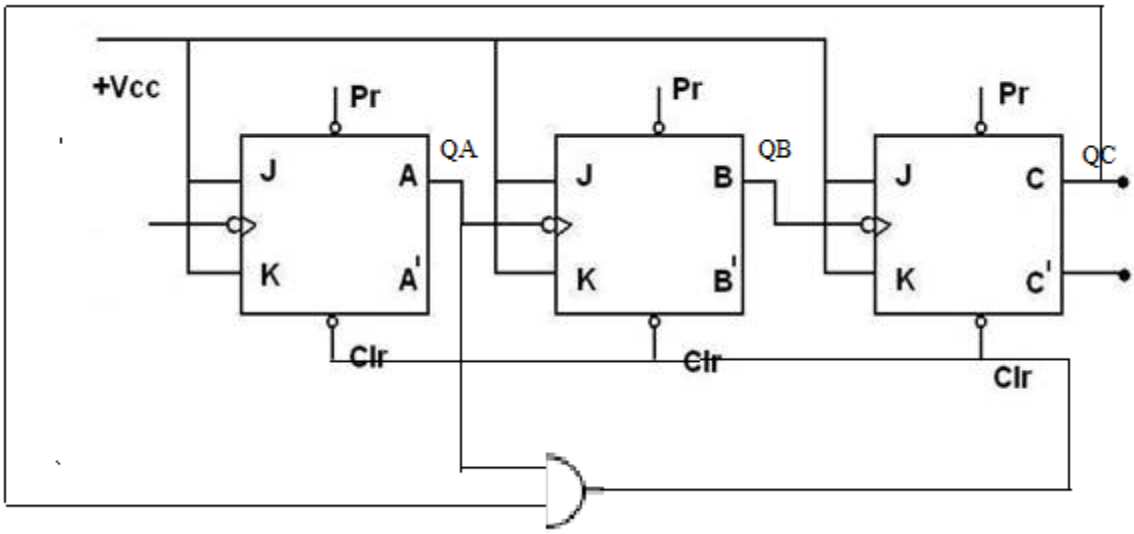
**CIRCUIT DIAGRAMS:-**

**1. 3 BIT RIPPLE COUNTER**




**2. MOD 5 RIPPLE COUNTER**

A counter which is reset at the fifth clock pulse is called Mod 5 counter or Divide by 5 counter. The circuit diagram of Mod 5 counter is shown in the figure. This counter contains three JK flip-flop.

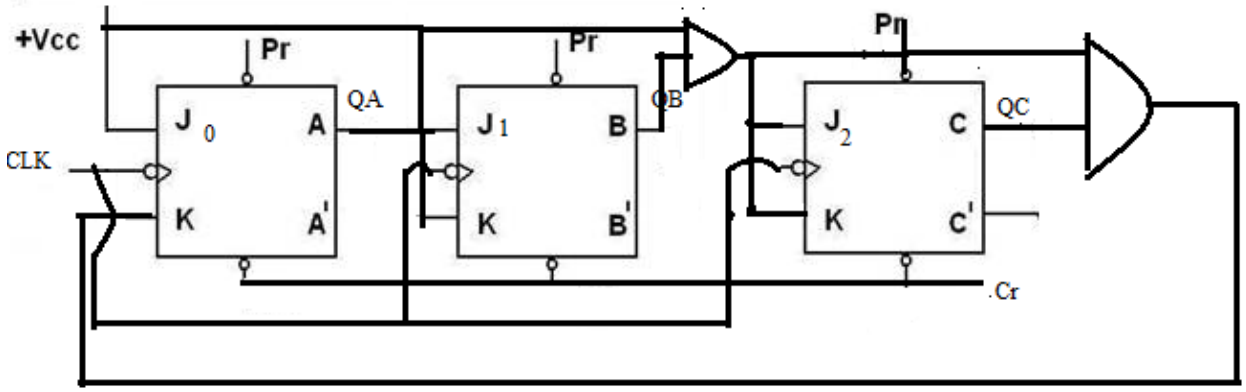


## 3. MOD 5 SYNCHRONOUS COUNTER

| Q2 Q1 Q0 | J0 K0 | J1 K1 | J2 K2 |
|---|---|---|---|
| 0 0 0 | 1 X | 0 X | 0 X |
| 0 0 1 | X 0 | 1 X | 0 X |
| 0 1 1 | X 0 | X 1 | 1 X |
| 1 0 1 | X 0 | 1 X | X 0 |
| 1 1 1 | X 1 | 1 X | X 1 |
| 0 0 0 | | | |

On simplification by using K-map

J0 =1; J1=QA; J2= QBQA;
K0=QCQBQA; K1=1; K2= QBQA;




## 4. IC 7490 DECADE COUNTER

| S no | Q3Q2Q1Q0 |
|---|---|
| 0 | 0 0 0 0 |
| 1 | 0 0 0 1 |
| 2 | 0 0 1 0 |
| 3 | 0 0 1 1 |
| 4 | 0 1 0 0 |
| 5 | 0 1 0 1 |
| 6 | 0 1 1 0 |
| 7 | 0 1 1 1 |
| 8 | 1 0 0 0 |
| 9 | 1 0 0 1 |
| | 0 0 0 0 |

**RESULT:-**

**POST LAB QUESTIONS:-**

1. What is decade counter?
2. How to design modulo-10 counter?
3. What is up-down counter?
4. What is a sequential circuit?
5. Differentiate between synchronous and asynchronous counter?
6. How many no.of flip-flops are required for decade counter?
7. What is meant by excitation table?
8. If the modulus of a counter is 12 how many flip-flops are required?

# EXPERIMENT-14

## MUX- DEMUX APPLICATIONS

**AIM: -**

1. To Realize a 4:1 MUX using basic gates.
2. To Realize a 1:4 MUX(De MUX) using basic gates.
3. To Realize the given logic expression using 8:1 MUX using IC 74151

   F(A,B,C,D)=Σ(2,4,5,7,10,12,14,15)
4. To Realize a Full Adder using 8:1 MUX (IC 74151)
5. To Realize a half Subs tractor using 4:1 MUX (IC 74153)

**APPARATUS REQUIRED:-**

1. ICS-IC 7408,IC 7432,IC 7404,IC 74151,IC 74153
2. Trainer kit & Connecting wires.

**THOERY:-**

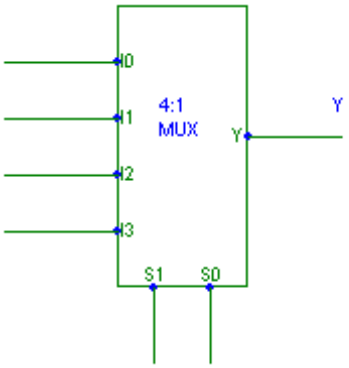
Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. A simple example of an non electronic circuit of a multiplexer is a single pole multiposition switch. Multiposition switches are widely used in many electronics circuits. However circuits that operate at high speed require the multiplexer to be automatically selected. A mechanical switch cannot perform this task satisfactorily. Therefore, multiplexer used to perform high speed switching are constructed of electronic components. Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates.The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output. Few types of multiplexer are 2-to-1, 4-to-1, 8-to-1, 16-to-1 multiplexer.

Multiplexer are used in various fields where multiple data need to be transmitted using a single line like Communication system, Telephone network, Computer memory and Transmission from the computer system of a satellite.Demultiplexer means one to many. A demultiplexer is a circuit with one input and many output. By applying control signal, we can steer any input to the output. Few types of demultiplexer are 1-to 2, 1-to-4, 1-to-8 and 1-to 16 demultiplexer. The main application area of demultiplexer is communication system where

multiplexer are used. Most of the communication system are bidirectional i.e. they function in both ways (transmitting and receiving signals). Hence, for most of the applications, the multiplexer and demultiplexer work in sync. Demultiplexer are also used for reconstruction of parallel data and ALU circuits.

## REALIZATION OF MUXS:-

### 1. 4:1 MUX

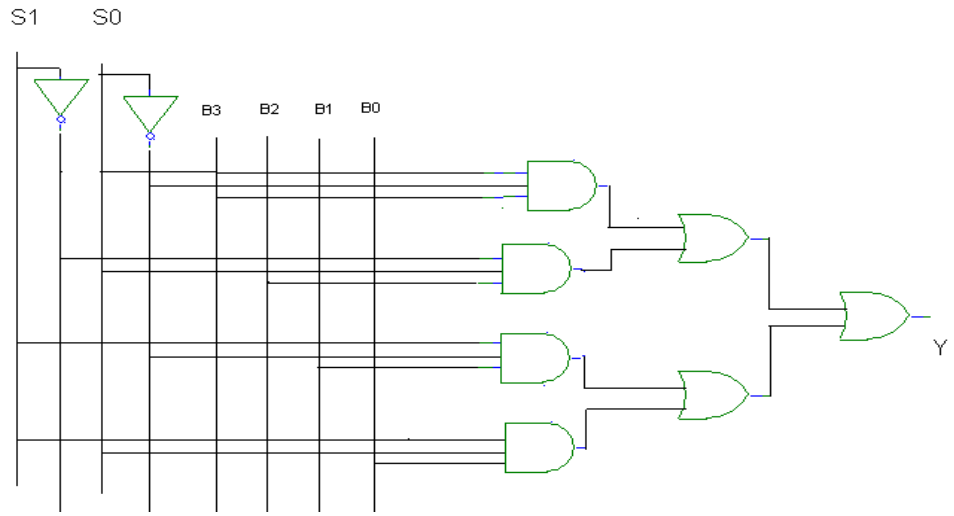



### TRUTH TABLE

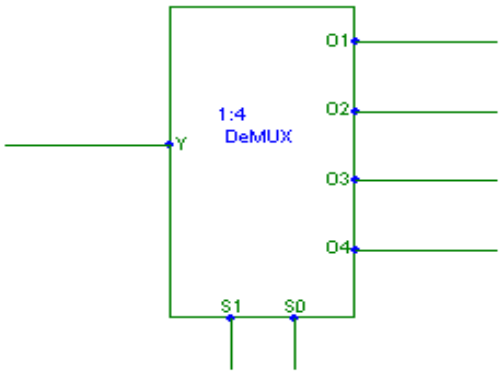
| En | **S1S0** | Y |
|---|---|---|
| I0 | **00** | I0 |
| I1 | **01** | I1 |
| I2 | **10** | I2 |
| I3 | **11** | I3 |

Y=S1'S0'I0+S1'S0I1+S1S0'I2+S1SoI3;

## CIRCUIT DIAGRAM:-



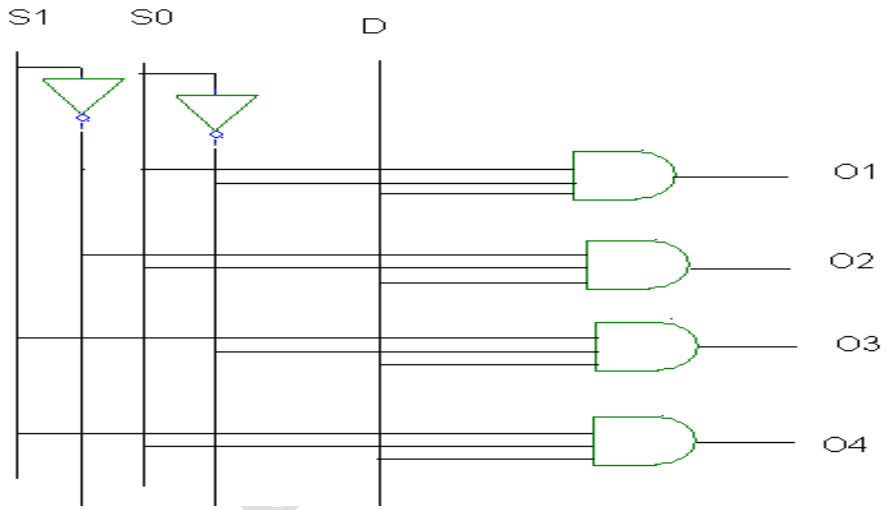
**2. 1:4 MUX:-**




**EQAUATIONS**

O1=S1'S0'D
O2=S1'S0D
O3=S1S0'D
O4=S1S0D;

**CIRCUIT DIAGRAM:-**

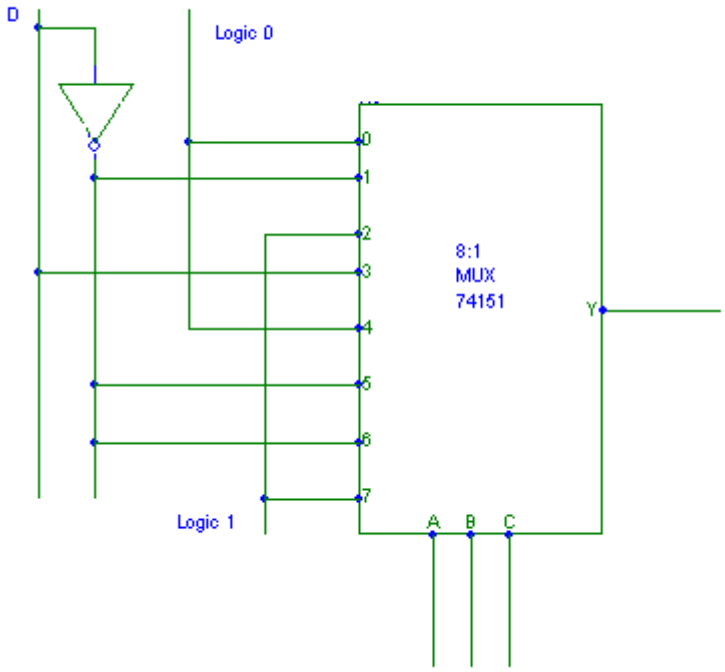


## 3. BOOLEAN EXPRESION

f(A,B,C,D)=Σ(2,4,5,7,10,12,14,15)

**TRUTH TABLE** **CIRCUIT DIAGRAM**

| ABCD | Y | ABC | Y |
|---|---|---|---|
| 0000 | 0 | 000 | 0 |
| 0001 | 1 | | |
| 0010 | 0 | 001 | D’ |
| 0011 | 1 | | |
| 0100 | 1 | 010 | 1 |
| 0101 | 0 | | |
| 0110 | 0 | 011 | D |
| 0111 | 1 | | |
| 1000 | 0 | 100 | 0 |
| 1001 | 0 | | |
| 1010 | 1 | 101 | D’ |
| 1011 | 0 | | |
| 1100 | 1 | 110 | D’ |
| 1101 | 0 | | |
| 1110 | 1 | 111 | 1 |
| | 1 | | |

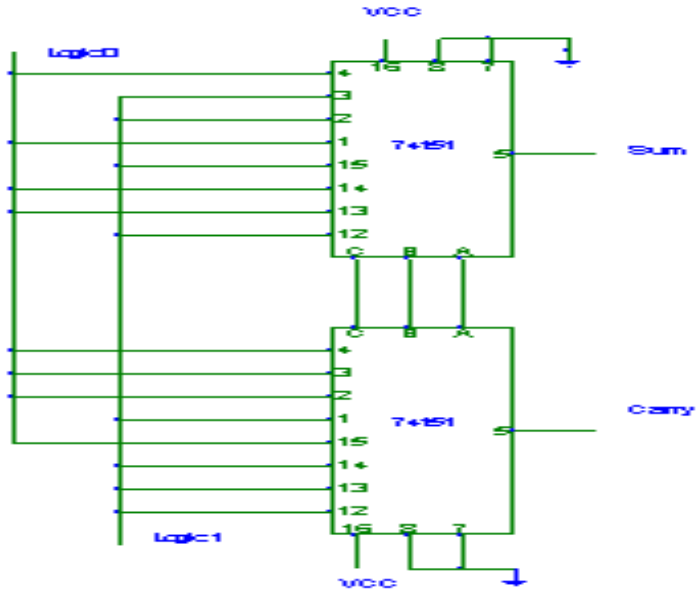



## 4.FULL ADDER USING 8:1 MUX (IC 74151):-

| CBA | S | C |
|---|---|---|
| 000 | 0 | 0 |
| 001 | 1 | 0 |
| 010 | 1 | 0 |
| 011 | 0 | 1 |
| 100 | 1 | 0 |
| 101 | 0 | 1 |
| 110 | 0 | 1 |
| 111 | 1 | 1 |

Sum= A’B’C+A’BC’+AB’C’+ABC
Carry=A’BC+AB”C+ABC

**CIRCUIT DIAGRAM**

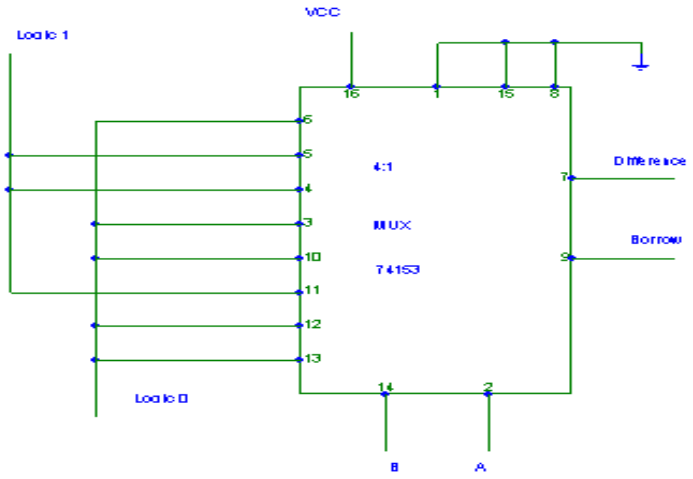



**6.HALF SUBTRACTOR USING IC 74153**

**TRUTH TABLE**

| AB | D | B |
|---|---|---|
| 00 | 0 | 0 |
| 01 | 1 | 1 |
| 10 | 1 | 0 |
| 11 | 0 | 0 |

**CIRCUIT DIAGRAM:-**



**PROCEDURE:-**

1. The Connections are made as per the circuit diagram.
2. By giving the different Binary inputs ,locate the output such that it matches with the function table of the MUX.
3. Repeat the same procedure for different circuits & take the outputs.

**RESULT: -** The realization of 4:1 MUX and DeMUX1:4 using basic gates & realization of given function ,full adder and half sub tractor is performed and the output is noted and practically verified.

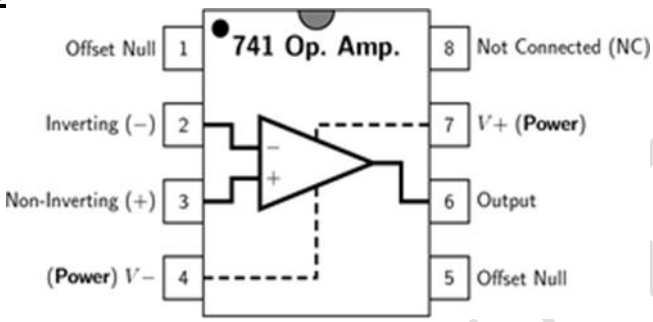
**POST LAB QUESTIONS :-**

1. What is meant by multiplexer?
2. What are applications of mux?
3. What is demultiplexer?
4. Design 8 input1 output multiplexer?
5. How many 8X1 multiplexers are needed to construct 16X1 multiplexer?
6. Compare decoder with demultiplexer?
7. Design a full adder using 8X1 multiplexer?

## APPENDIX – A

### 1.IC 741

**Pin Configuration:**

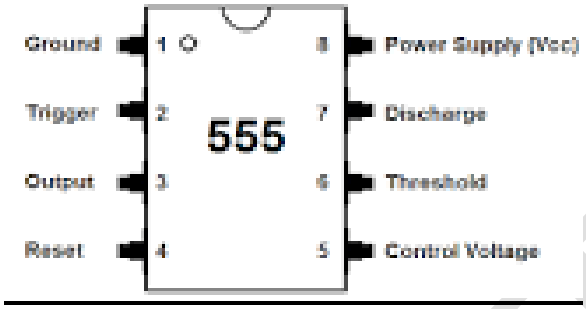



**Specifications:**

1. Voltage gain A = α typically 2,00,000
2. I/P resistance RL = α Ω, practically 2MΩ
3. O/P resistance R1 =0, practically 75Ω
4. Bandwidth = α Hz. It can be operated at any frequency
5. Common mode rejection ratio = α
(Ability of op amp to reject noise voltage)
6. Slew rate + α V/µsec
(Rate of change of O/P voltage)
7. When V1 = V2, VD=0
8. Input offset voltage (Rs ≤ 10KΩ) max 6 mv
9. Input offset current = max 200nA
10. Input bias current : 500nA
11. Input capacitance : type value 1.4PF
12. Offset voltage adjustment range : ± 15mV
13. Input voltage range : ± 13V
14. Supply voltage rejection ratio : 150 µr/V
15. Output voltage swing: + 13V and – 13V for RL > 2KΩ
16. Output short-circuit current: 25mA
17. supply current: 28mA
18. Power consumption: 85MW
19. Transient response: rise time= 0.3 µs
Overshoot= 5%

## 2.IC 555

**Pin Configuration:**

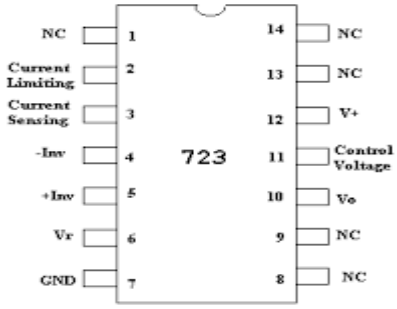



**Specifications:**

1. Operating temperature : SE 555 -55oC to 125oC
   NE 555 0o to 70oC
2. Supply voltage : +5V to +18V
3. Timing : µSec to Hours
4. Sink current : 200mA
5. Temperature stability : 50 PPM/oC change in temp or 0-005% /oC.

## 3. IC723

**Pin Configuration:**




**Specifications of 723:**

1. Power dissipation : 1W
2. Input Voltage : 9.5 to 40V
3. Output Voltage : 2 to 37V
4. Output Current : 150mA for Vin-Vo = 3V
5. 10mA for Vin-Vo = 38V
6. Load regulation : 0.6% Vo

Line regulation : 0.5% Vo

## APPENDIX B

## LABORATORY COURSE ASSESSMENT GUIDELINES

i. The number of experiments in each laboratory course shall be as per the curriculum in the scheme of instructions provided by OU. Mostly the number of experiments is 10 in each laboratory course under semester scheme and 18 under year wise scheme.

ii. The students will maintain a separate note book for observations in each laboratory course.

iii. In each session the students will conduct the allotted experiment and enter the data in the observation table.

iv. The students will then complete the calculations and obtain the results. The course coordinator will certify the result in the same session.

v. The students will submit the record in the next class. The evaluation will be continuous and not cycle-wise or at semester end.

vi. The internal marks of 25 are awarded in the following manner:

a. Laboratory record - Maximum Marks 15
b. Test and Viva Voce - Maximum Marks 10

vii. Laboratory Record: Each experimental record is evaluated for a score of 50. **The rubric parameters are as follows:**

a. Write up format - Maximum Score 15
b. Experimentation Observations & Calculations - Maximum Score 20
c. Results and Graphs - Maximum Score 10
d. Discussion of results - Maximum Score 5

While (a), (c) and (d) are assessed at the time of record submission, (b) is assessed during the session based on the observations and calculations. Hence if a student is absent for an experiment but completes it in another session and subsequently submits the record, it shall be evaluated for a score of 30 and not 50.

viii. The experiment evaluation rubric is therefore as follows:

| Parameter | Max Score | Outstanding | Accomplished | Developing | Beginner | Points |
|---|---|---|---|---|---|---|
| Observations and Calculations | 20 | | | | | |
| Write up format | 15 | | | | | |
| Results and graphs | 10 | | | | | |
| Discussion of Results | 5 | | | | | |

**LABORATORY EXPERIMENT EVALUATION RUBRIC**

| CATEGORY | OUTSTANDING (Up to 100%) | ACCOMPLISHED (Up to 75%) | DEVELOPING (Up to 50%) | BEGINNER (Up to 25%) |
|---|---|---|---|---|
| Write up format | Aim, Apparatus, material requirement, theoretical basis, procedure of experiment, sketch of the experimental setup etc. is demarcated and presented in clearly labeled and neatly organized sections. | The write up follows the specified format but a couple of the specified parameters are missing. | The report follows the specified format but a few of the formats are missing and the experimental sketch is not included in the report | The write up does not follow the specified format and the presentation is shabby. |
| Observations and Calculations | The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures. One sample calculation is explained by substitution of values | The experimental observations and calculations are recorded in neatly prepared table with correct units and significant figures but sample calculation is not shown | The experimental observations and calculations are recorded neatly but correct units and significant figures are not used. Sample calculation is also not shown | The experimental observations and results are recorded carelessly. Correct units significant figures are not followed and sample calculations not shown |
| Results and Graphs | Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations are performed from the graphs. Equations are obtained by regression analysis or curve fitting if relevant | Results obtained are correct within reasonable limits. Graphs are drawn neatly with labeling of the axes. Relevant calculations from the graphs are incomplete and equations are not obtained by regression analysis or curve fitting | Results obtained are correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting | Results obtained are not correct within reasonable limits. Graphs are not drawn neatly and or labeling is not proper. No calculations are done from the graphs and equations are not obtained by regression analysis or curve fitting |
| Discussion of results | All relevant points of the result are discussed and justified in light of theoretical expectations. Reasons for divergent results are identified and corrective measures discussed. | Results are discussed but no theoretical reference is mentioned. Divergent results are identified but no satisfactory reasoning is given for the same. | Discussion of results is incomplete and divergent results are not identified. | Neither relevant points of the results are discussed nor divergent results identified |

ix. The first page of the record will contain the following title sheet:

**SAMPLE ASSESSMENT SHEET**

**NAME:** **ROLL NO.**

| Exp. No. | Date conducted | Date Submitted | Observations &Calculations (Max 20) | Write up (Max 15) | Results and Graphs (Max 10) | Discussion of Results (Max 5) | Total Score (Max 50) |
|---|---|---|---|---|---|---|---|
| 1 | | | | | | | |
| 2 | | | | | | | |
| 3 | | | | | | | |
| 4 | | | | | | | |
| 5 | | | | | | | |
| 6 | | | | | | | |
| 7 | | | | | | | |
| 8 | | | | | | | |
| 9 | | | | | | | |
| 10 | | | | | | | |
| 11 | | | | | | | |
| 12 | | | | | | | |



x. The 15 marks of laboratory record will be scaled down from the TOTAL of the assessment sheet.

xi. The test and viva voce will be scored for 10 marks as follows:

| | | |
|---|---|---|
| Internal Test | - | 6 marks |
| Viva Voce / Quiz | - | 4 marks |

xii. Each laboratory course shall have 5 course outcomes.

**The proposed course outcomes are as follows:**

On successful completion of the course, the student will acquire the ability to:

1. Conduct experiments, take measurements and analyze the data through hands-on experience in order to demonstrate understanding of the theoretical concepts of _____, while working in small groups.

2. Demonstrate writing skills through clear laboratory reports.

3. Employ graphics packages for drawing of graphs and use computational software for statistical analysis of data.

4. Compare the experimental results with those introduced in lecture, draw relevant conclusions and substantiate them satisfactorily.

5. Transfer group experience to individual performance of experiments and demonstrate effective oral communication skills.

xiii. The Course coordinators would prepare the assessment matrix in accordance with the guidelines provided above for the five course outcomes. The scores to be entered against each of the course outcome would be the sum of the following as obtained from the assessment sheet in the record:

   a. Course Outcome 1: Sum of the scores under 'Observations and Calculations'.
   b. Course Outcome 2: Sum of the scores under 'Write up'.
   c. Course Outcome 3: Sum of the scores under 'Results and Graphs'.
   d. Course Outcome 4: Sum of the scores under 'Discussion of Results'.
   e. Course Outcome 5: Marks for 'Internal Test and Viva voce'.

xiv. Soft copy of the assessment matrix would be provided to the course coordinators.

**MUFFAKHAM JAH COLLEGE OF ENGINEERING AND TECHNOLOGY**

## Program Outcomes of B.E (ECE) Program:

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal, and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO 12: Life-long learning: Recognise the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

## Program Specific Outcomes (PSOs) of ECE Department, MJCET

PSO1: The ECE Graduates will acquire state of art analysis and design skills in the areas of digital and analog VLSI Design using modern CAD tools.

PSO2: The ECE Graduates will develop preliminary skills and capabilities necessary for embedded system design and demonstrate understanding of its societal impact.

PSO3: The ECE Graduates will obtain the knowledge of the working principles of modern communication systems and be able to develop simulation models of components of a communication system.

PSO4: The ECE Graduates will develop soft skills, aptitude and programming skills to be employable